Introduction to hardware design with Vivado Design Suite

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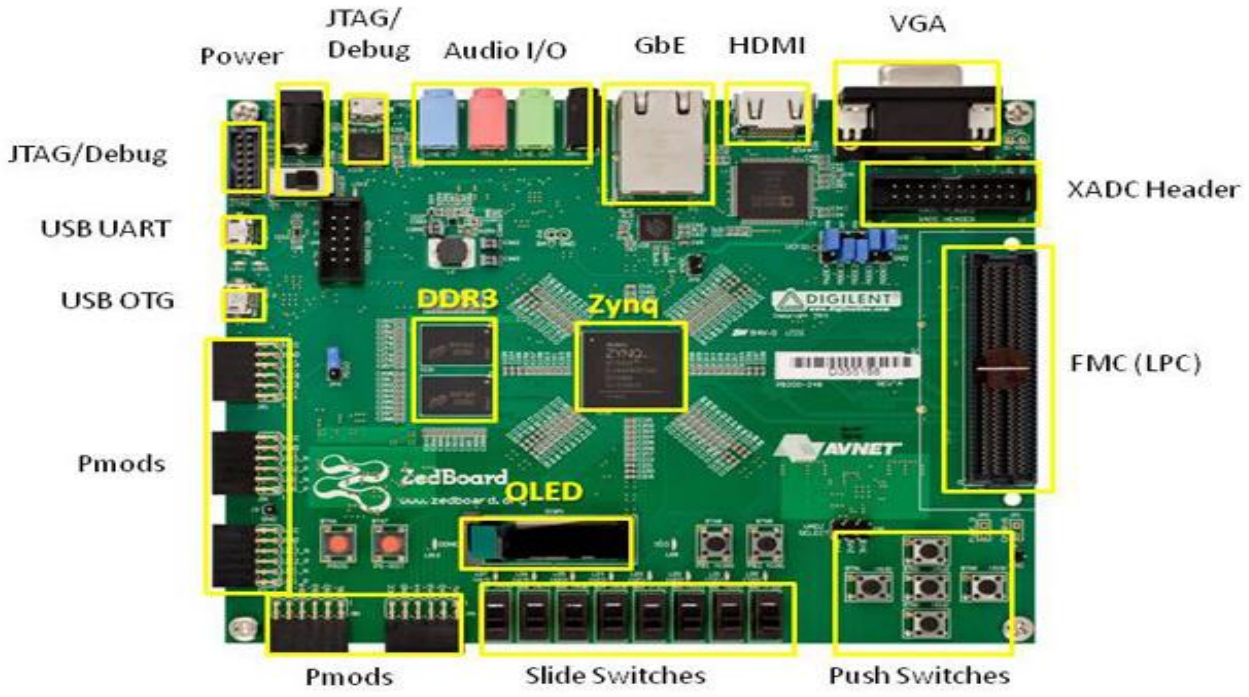
CS-220 (Spring ‘23)

FPGAs

- A Field Programmable Gate Array is a re-configurable circuit
- Hardware Description Languages (HDLs)



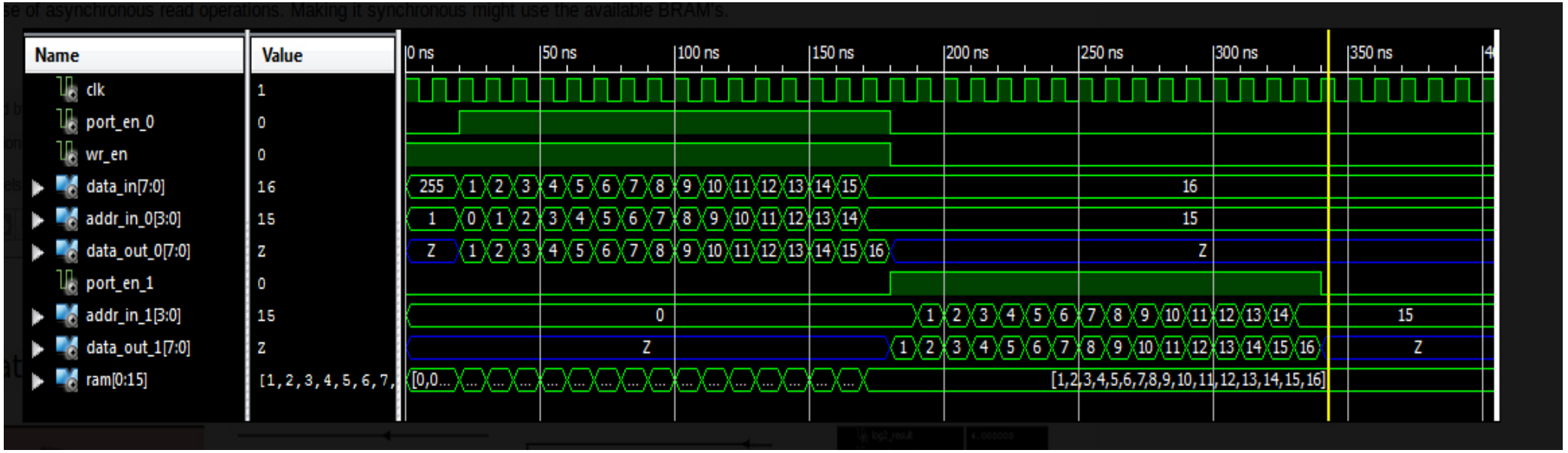
* SD card cage and OSPI Flash reside on backside of board

Vivado Design Suite

- Developed by Xilinx (now AMD)
- Vivado is suitable for
  - Simulation
  - Synthesis
- of HDL (SystemVerilog) designs

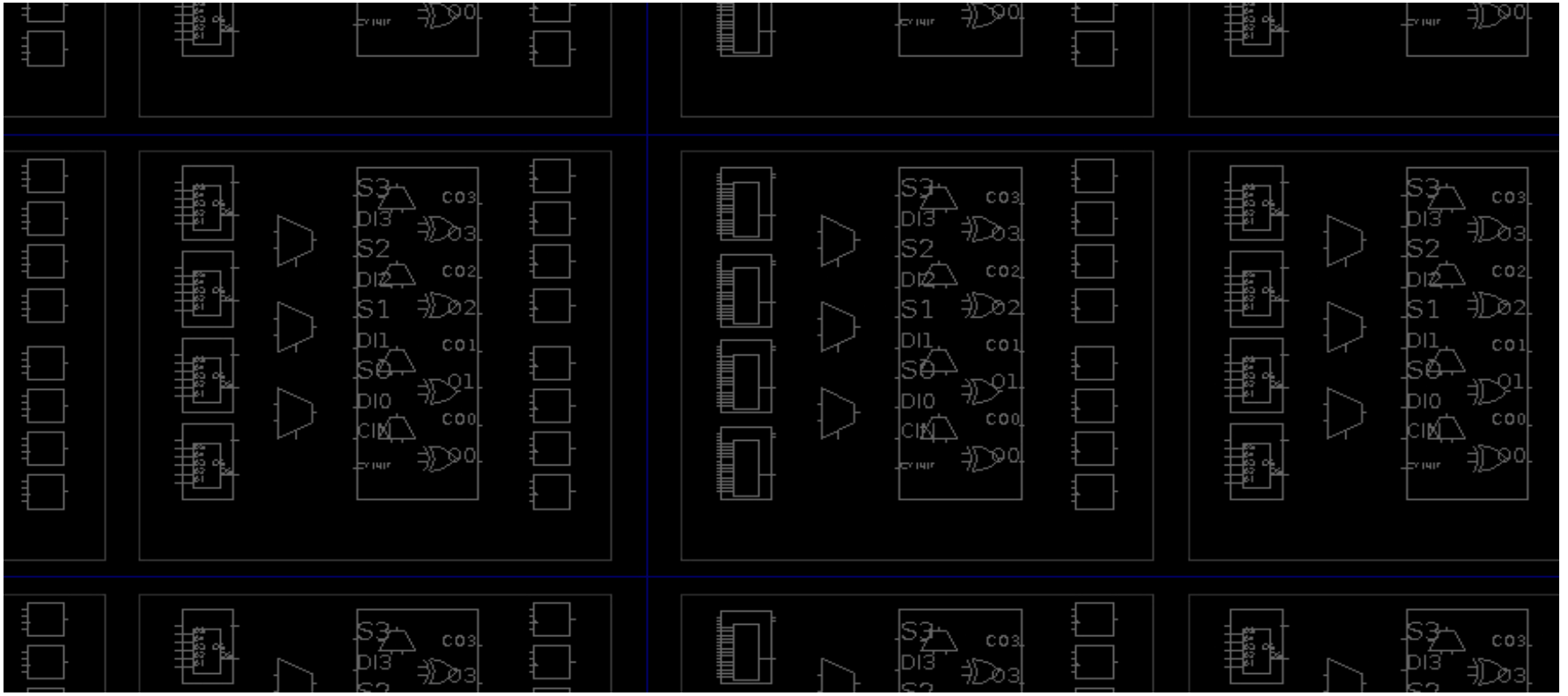
Simulation

- The simulation of a circuit displays circuit's behavior to hardware (HW) designers
- Why do we need a testbench (TB) for that?



Synthesis

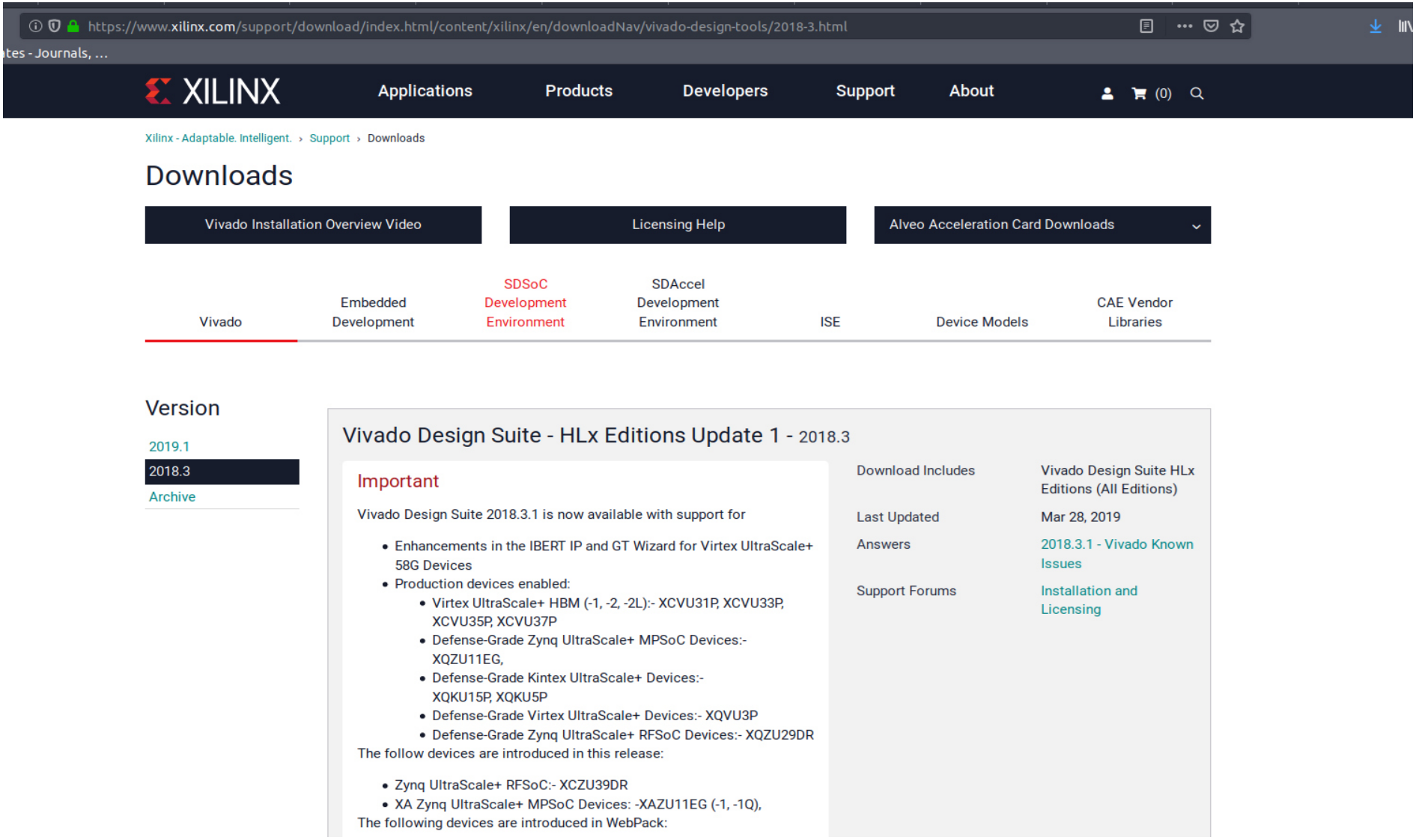
- Transforms Register Transfer Level (RTL) designs to logic gates
- Look-Up Tables (LUTs)



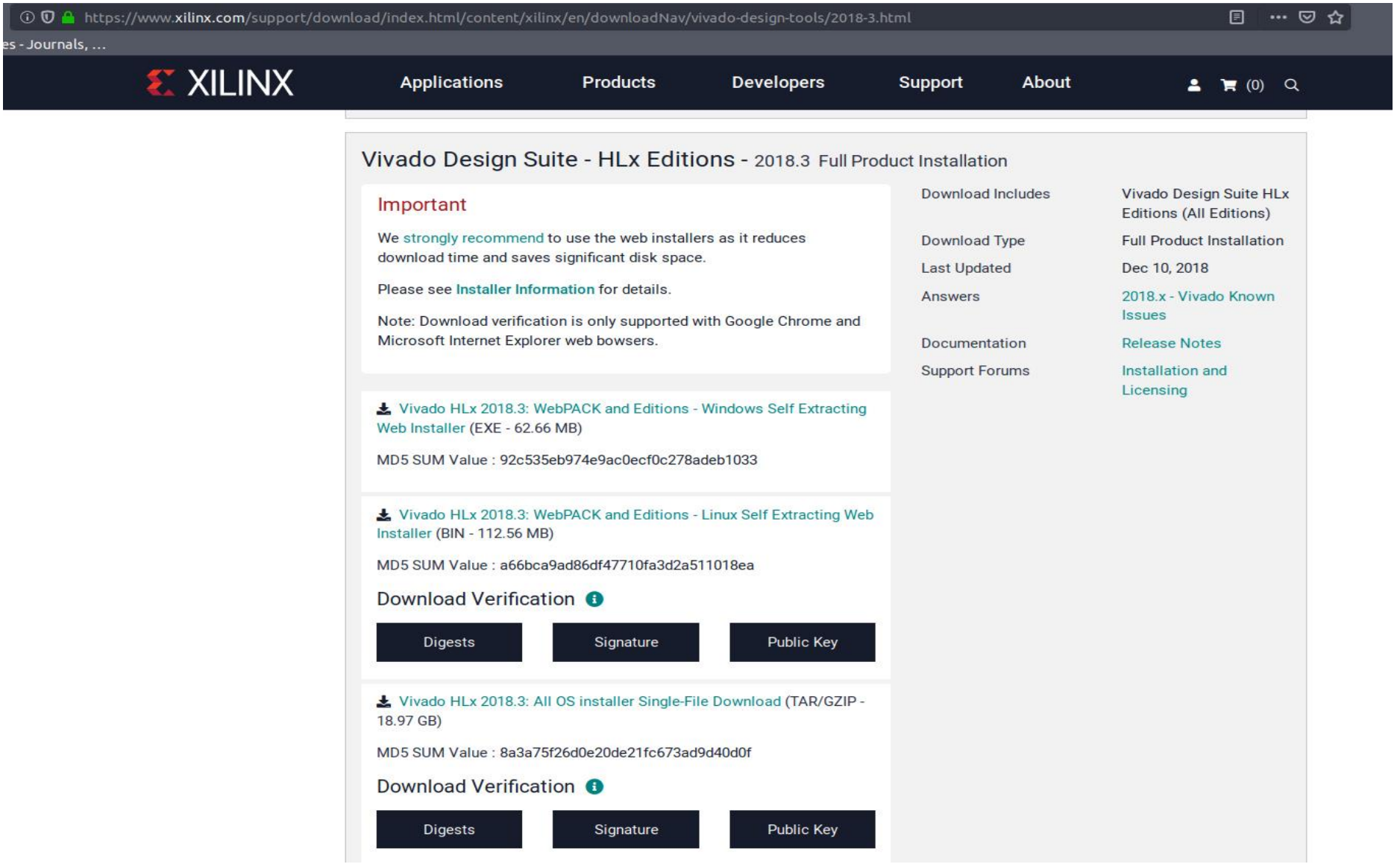
Vivado Installation

- Dependencies (especially) for Linux machines
  - sudo apt install libtinfo5
  - sudo apt install libncurses5
- Linux installation
  - chmod +x Xilinx_Vivado_Install.bin
  - (sudo) ./Xilinx_Vivado_Install.bin

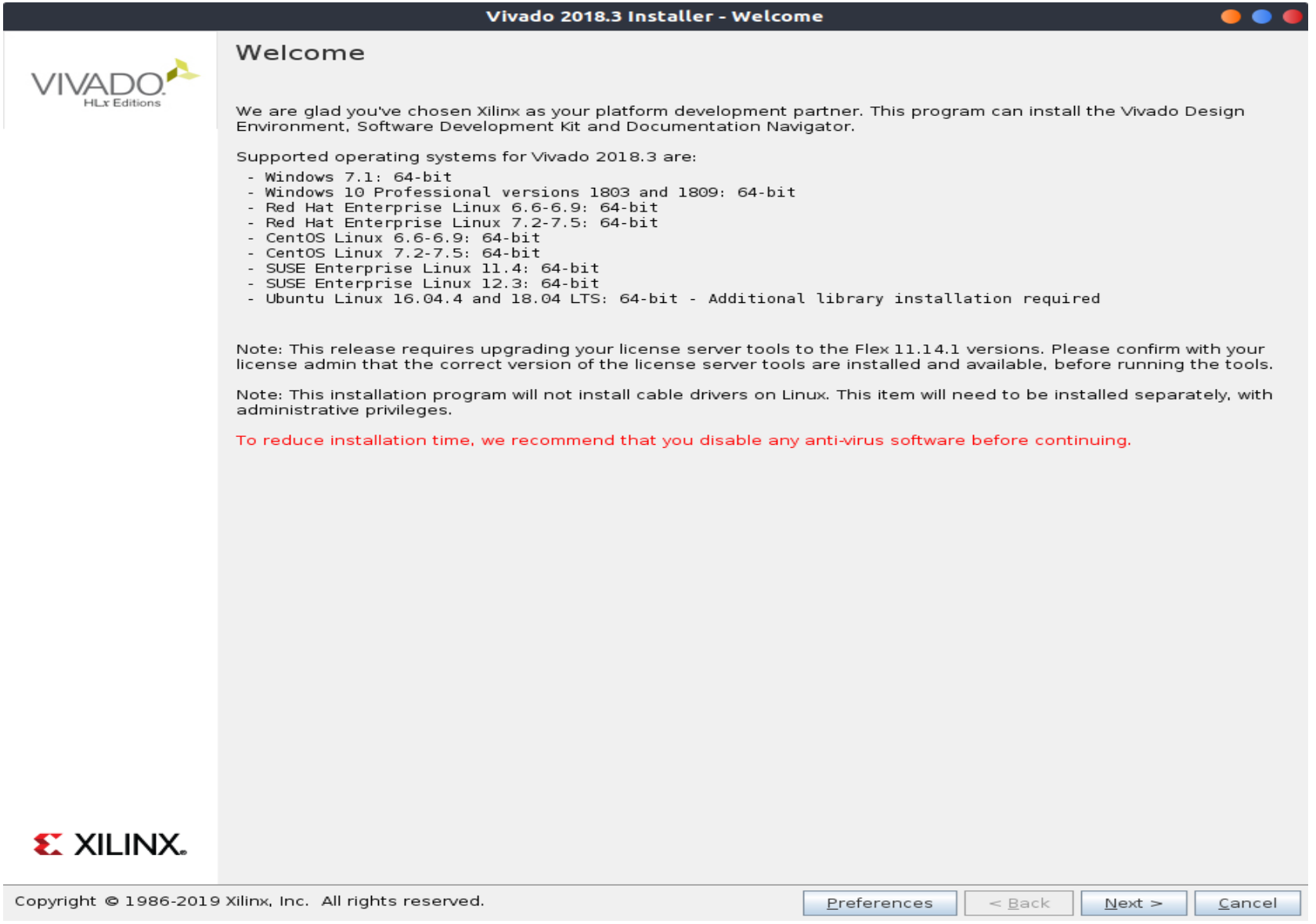
Vivado Installation (cont'd)



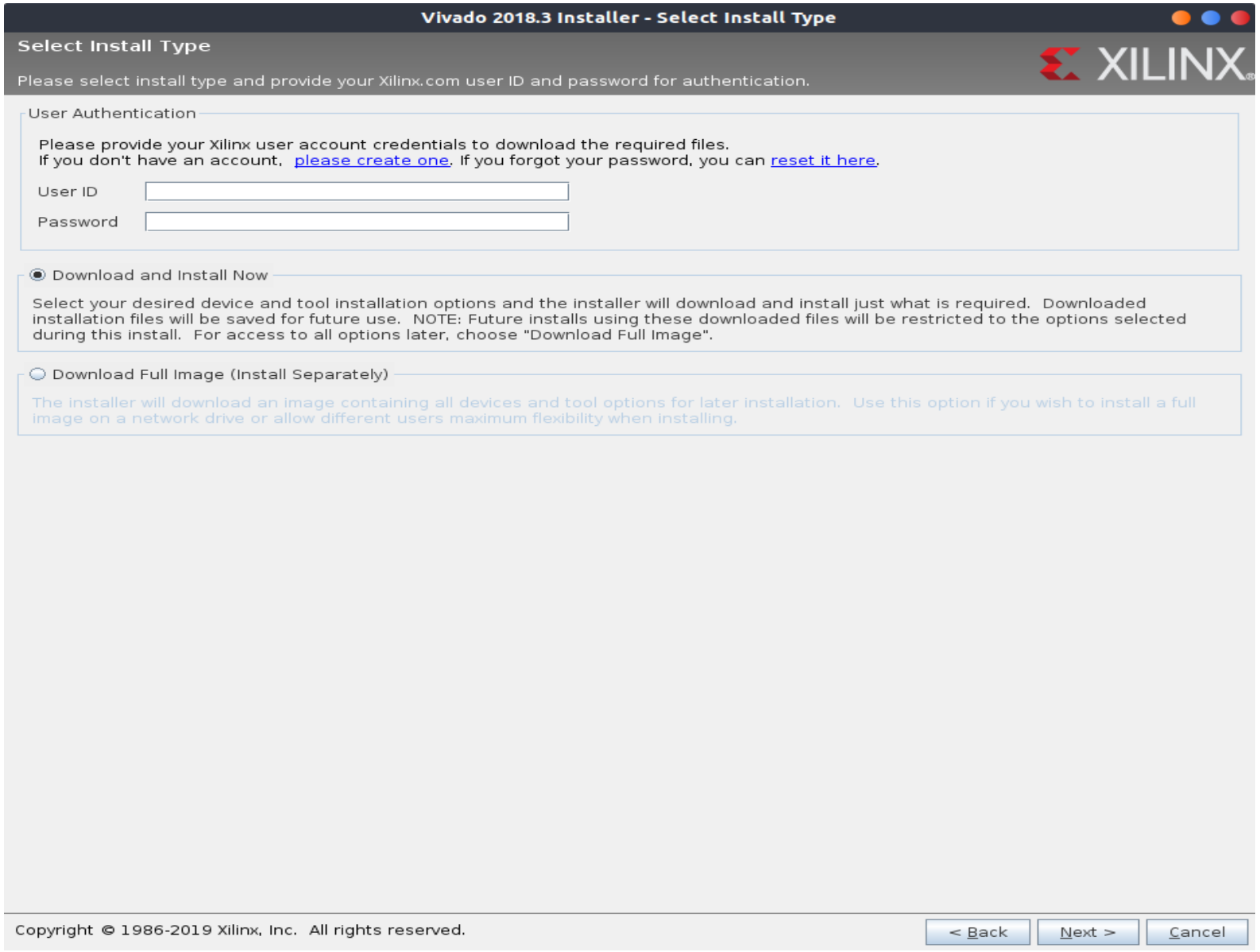
Vivado Installation (cont'd)



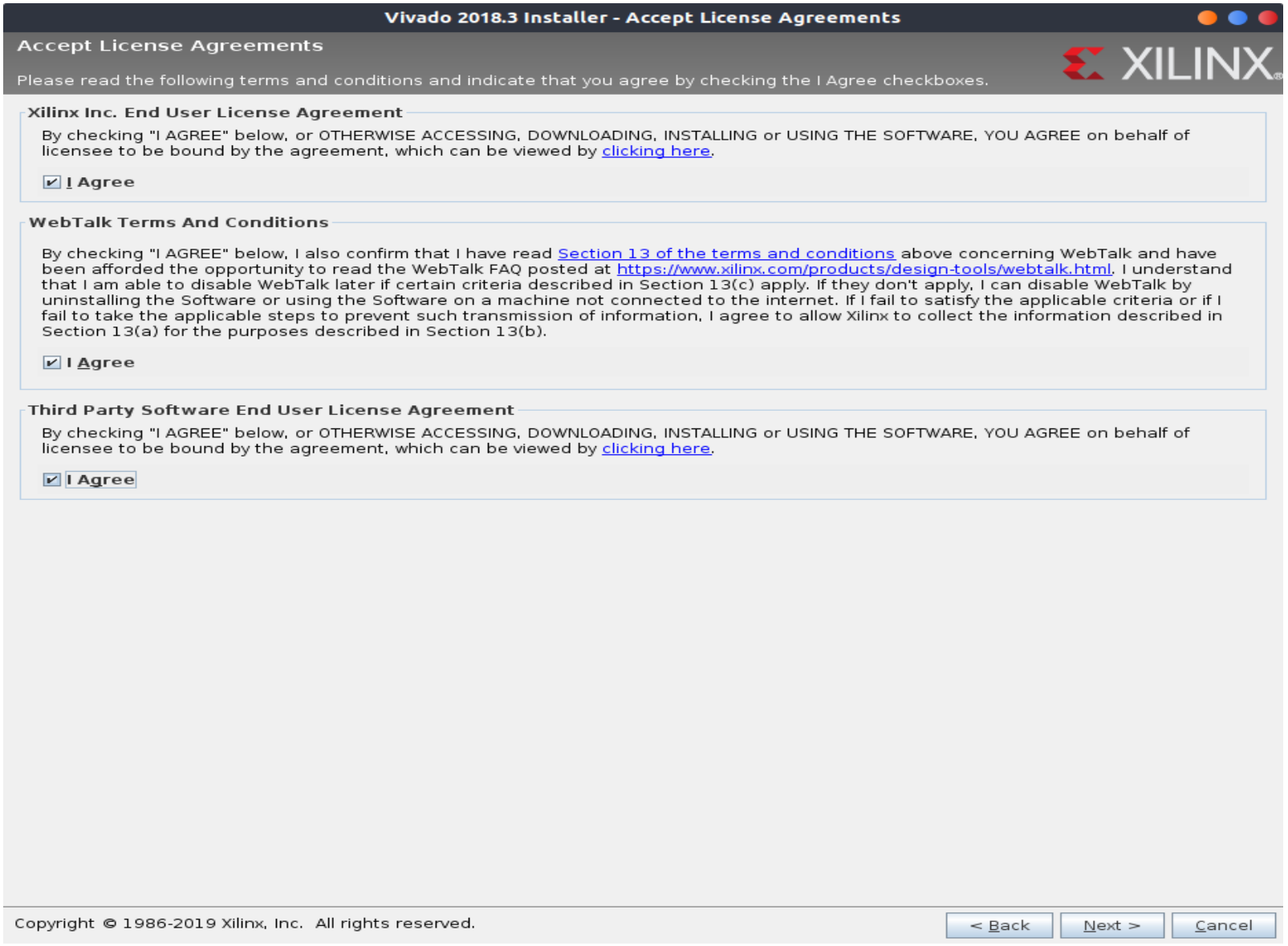
Vivado Installation (cont'd)



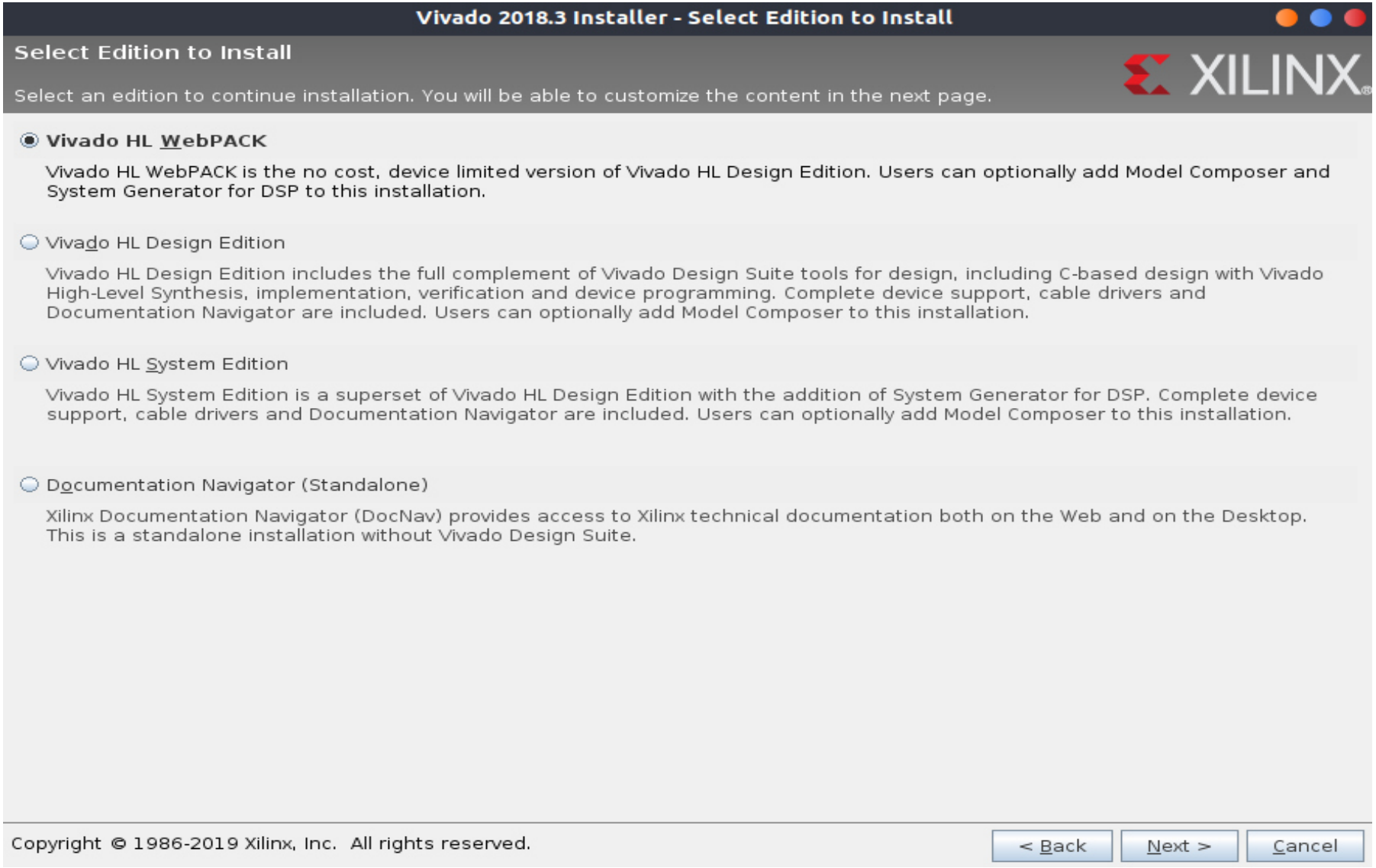
Vivado Installation (cont'd)



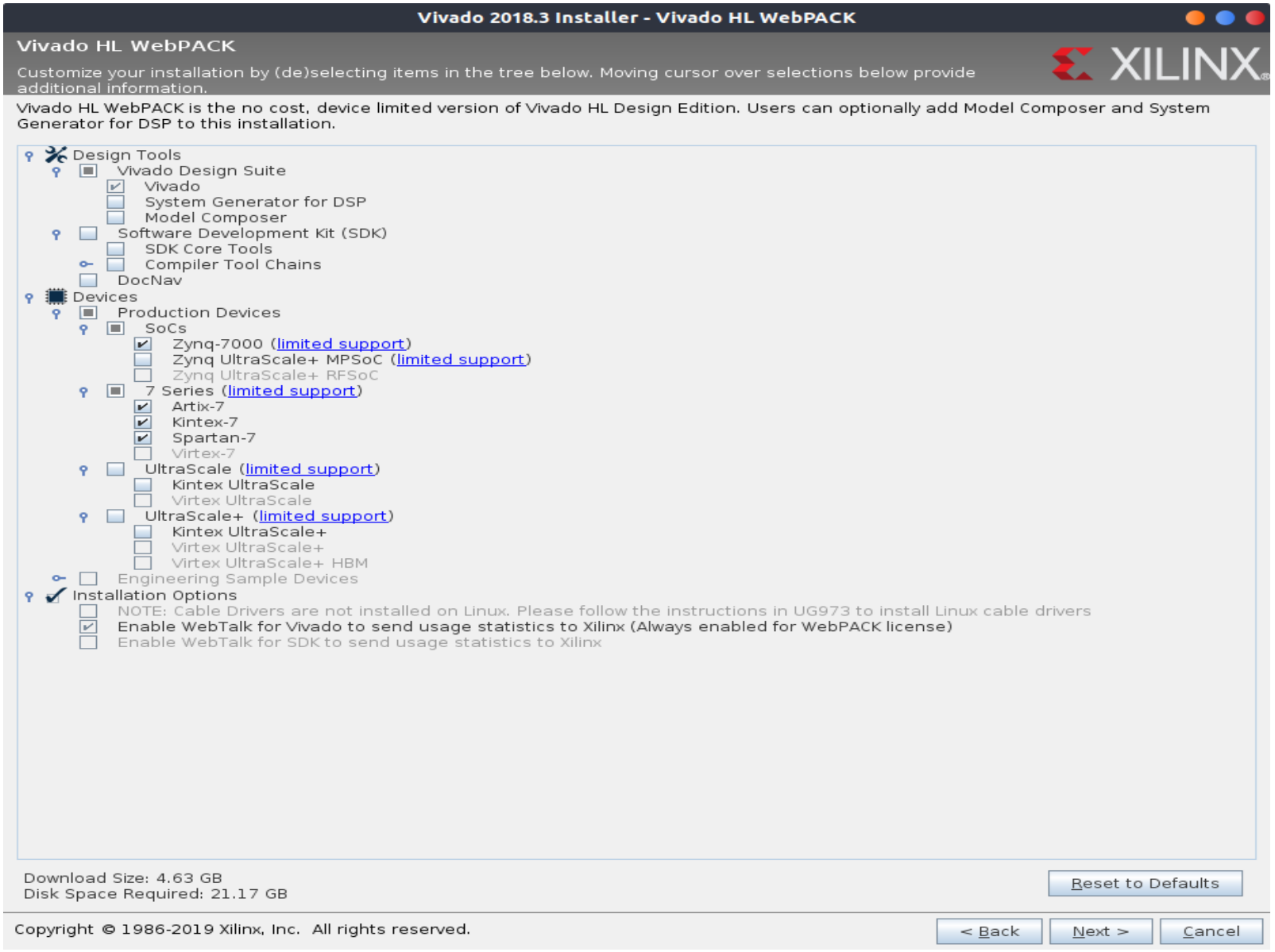
Vivado Installation (cont'd)



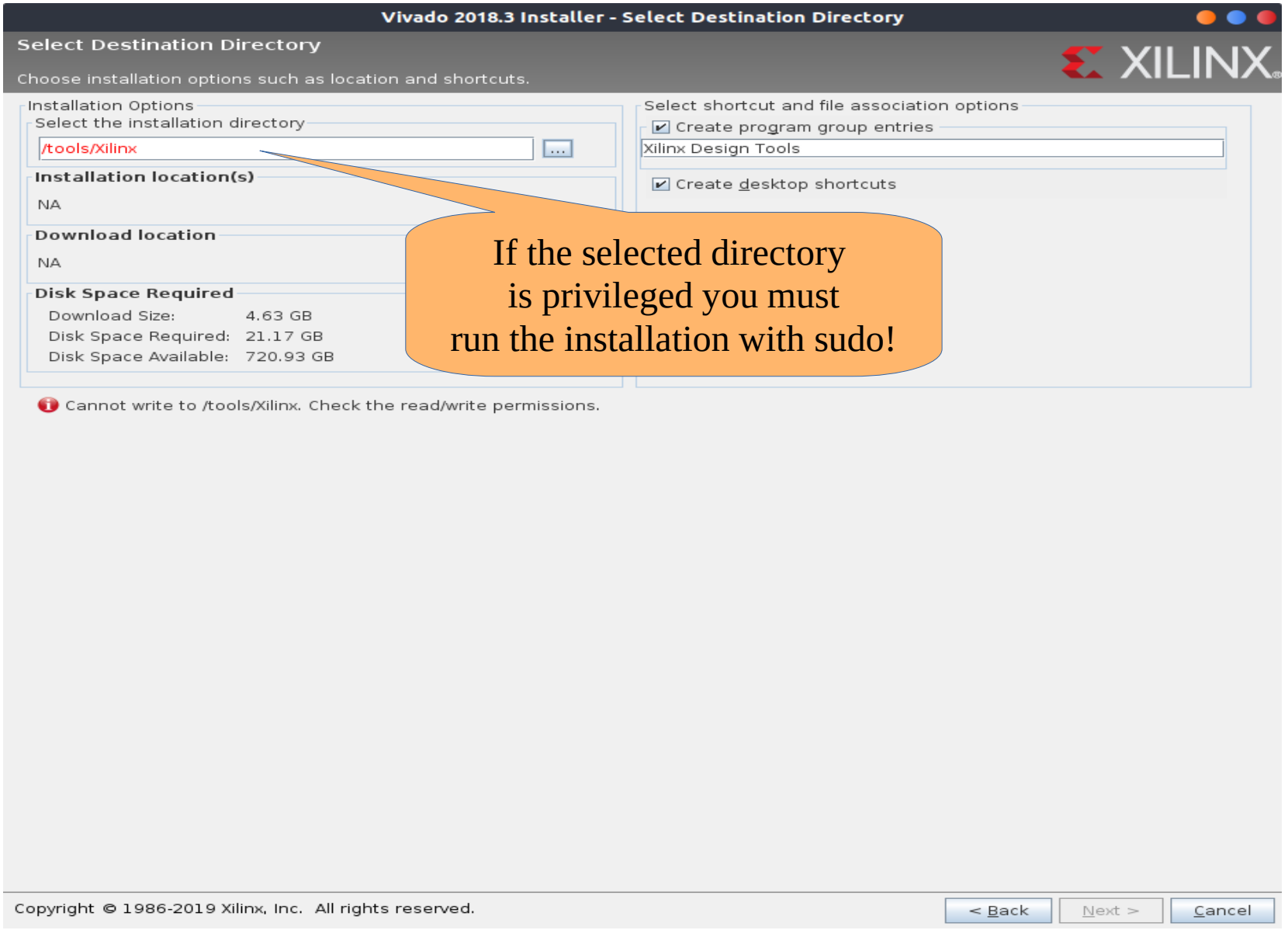
Vivado Installation (cont'd)



Vivado Installation (cont'd)



Vivado Installation (cont'd)



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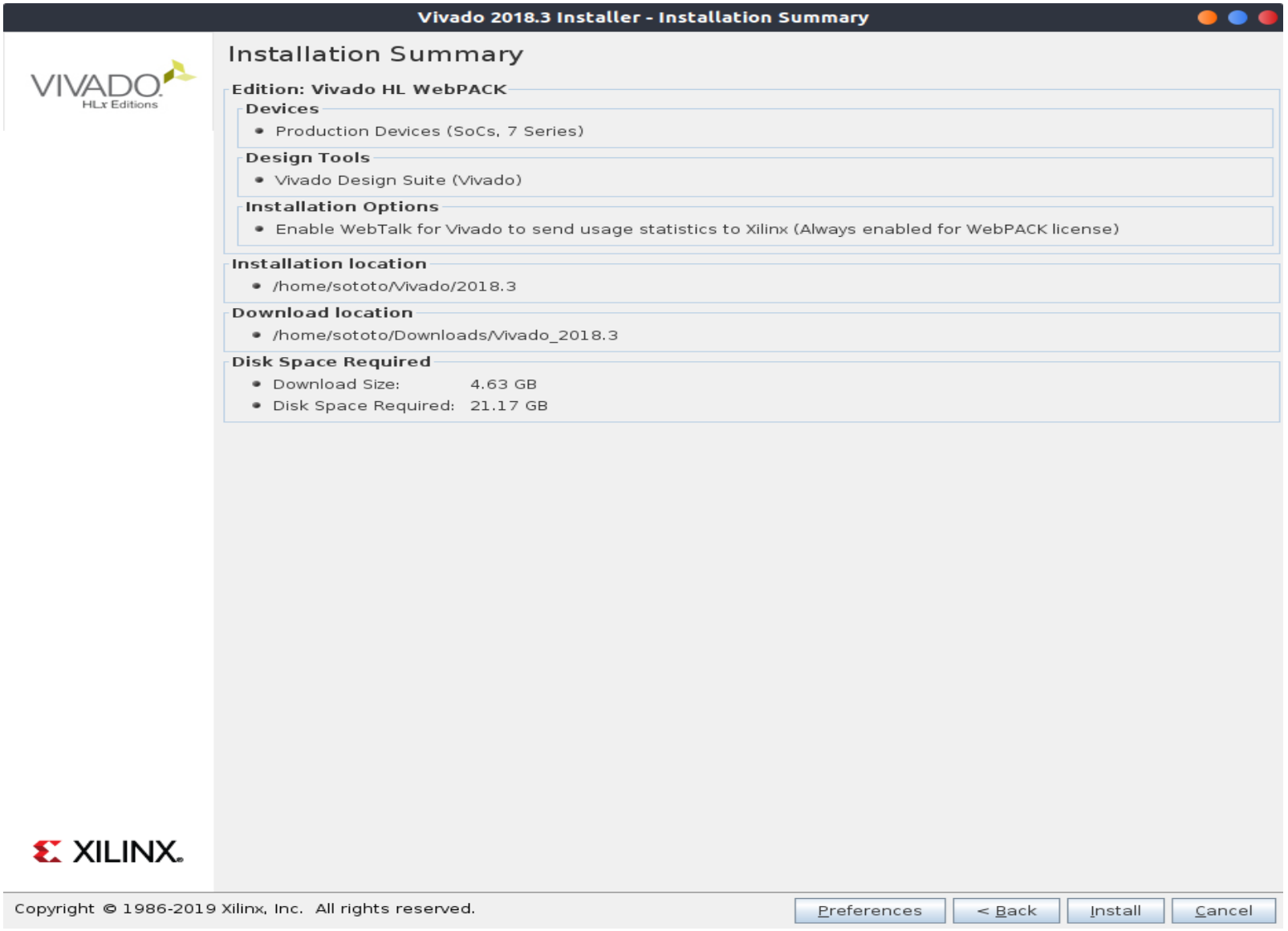


And… an alternative

- Instead of working on your own machine, you can run Vivado on Debian machines.
  - Interactively through command line
  - Interactively with GUI through ssh display forwarding (ssh -X <hostname>)

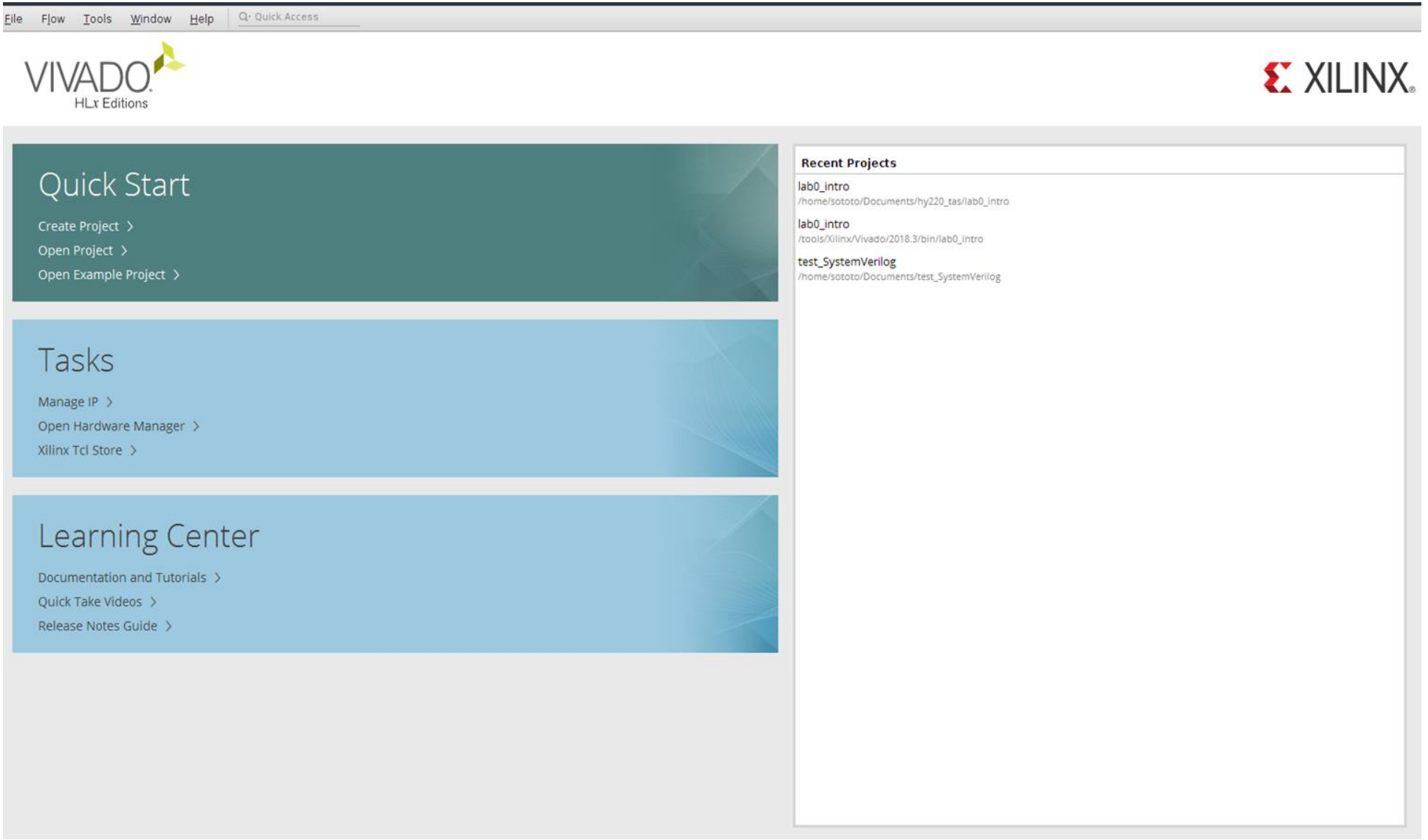
And… an alternative

- cp -r ~hy220/tools/example .
- source ~hy220/tools/setup.sh
- export LC_ALL="C"
- Work interactively
  - make (command line)
  - make waves (GUI-waves) (after make cmd)
  - make gui (GUI)

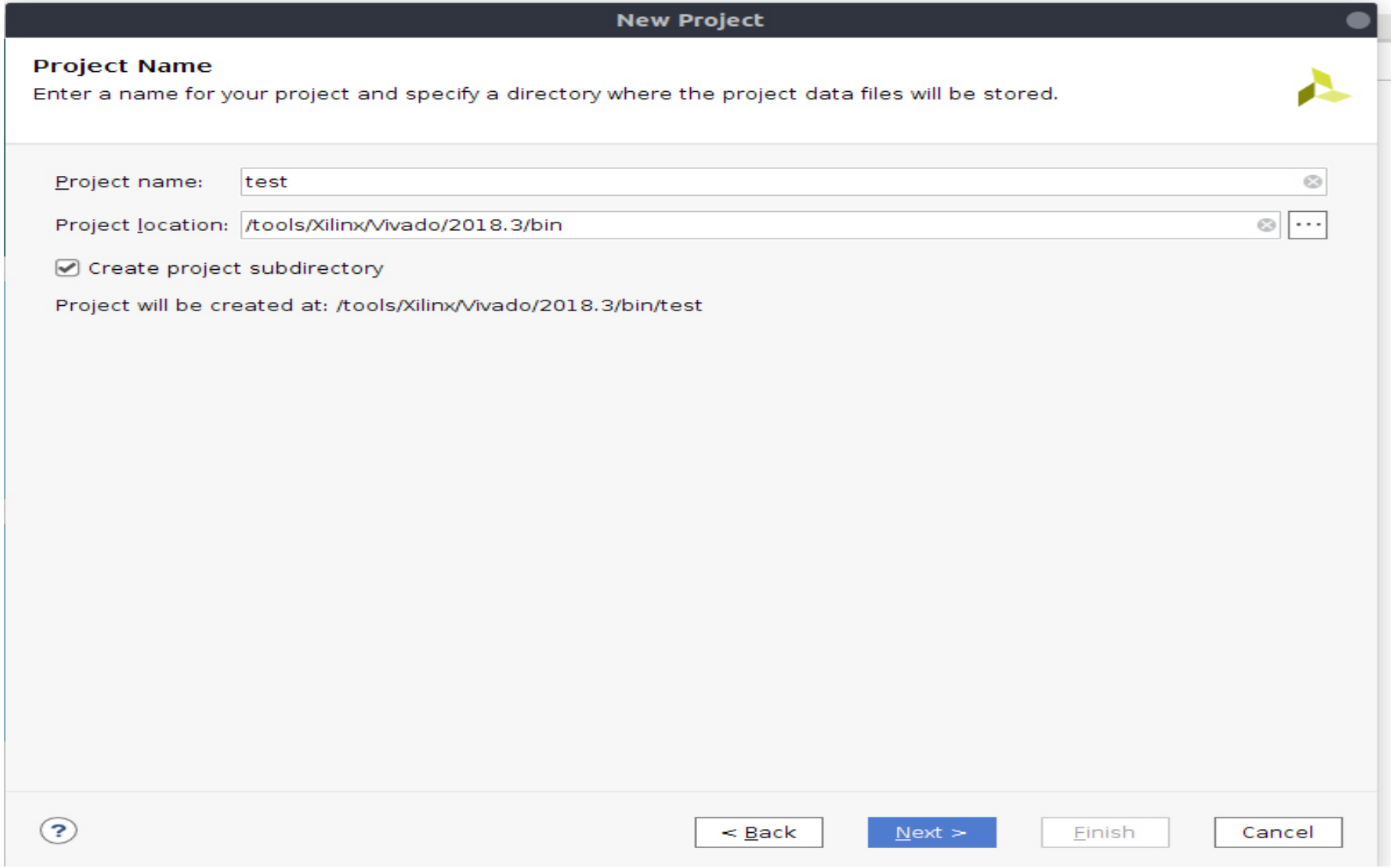
Sourcing settings to path

- Before executing Vivado through command line you have to source some already prepared settings
  - cd installation_path/Xilinx/Vivado/2018.3
  - source settings64.sh
- After this you can execute Vivado GUI by typing
  - vivado

Creating a project



Creating a project (cont'd)



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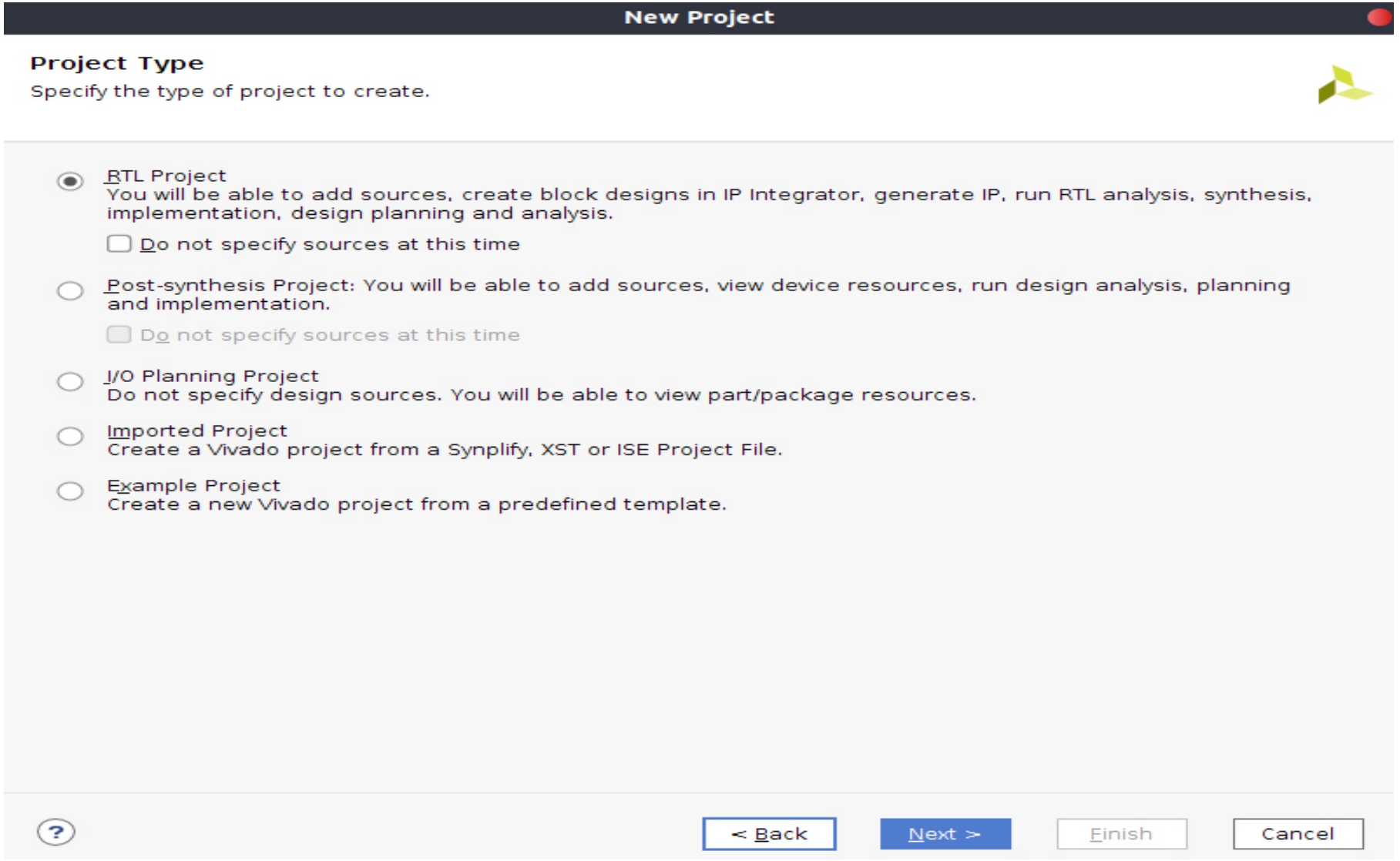

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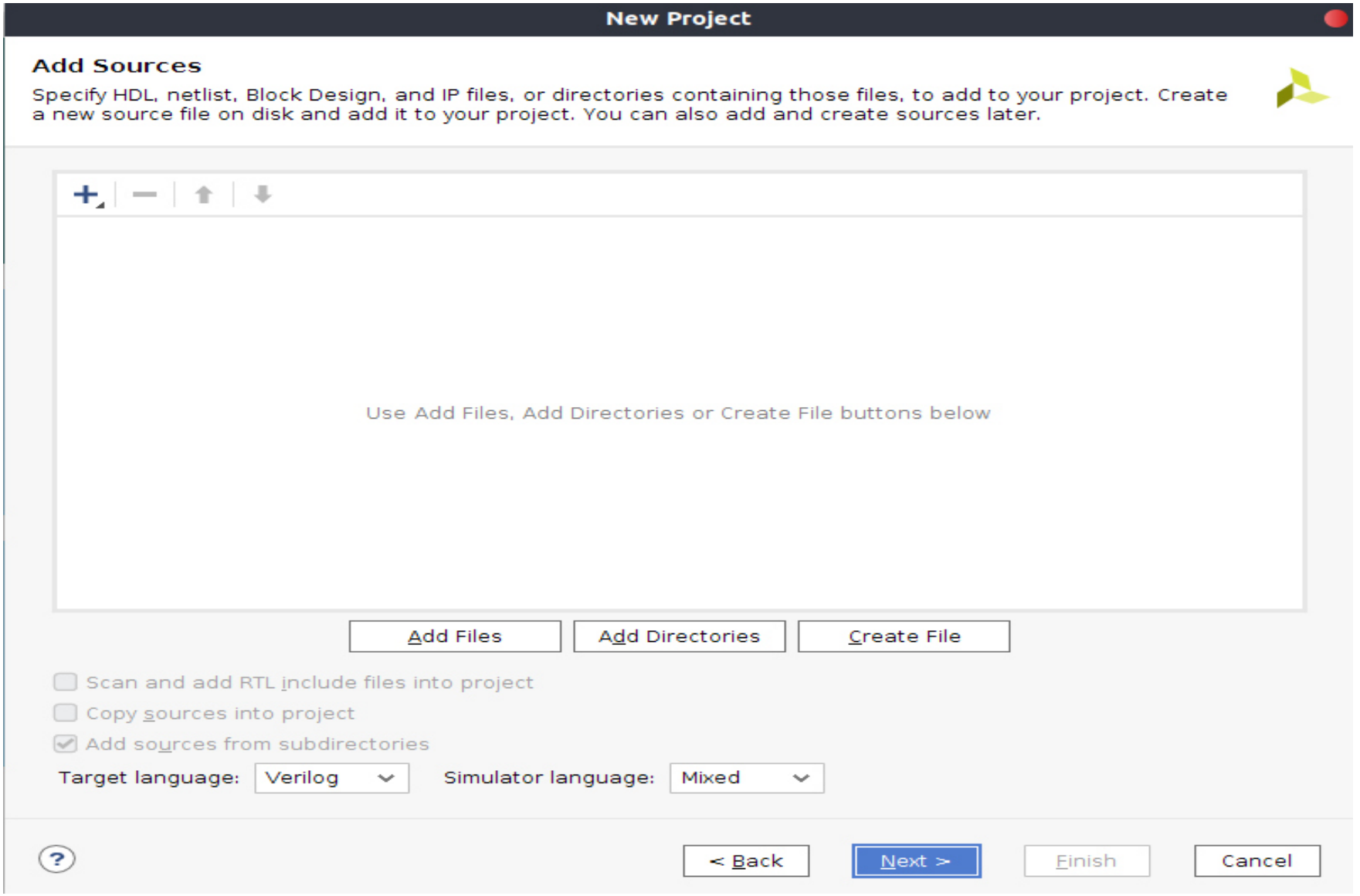

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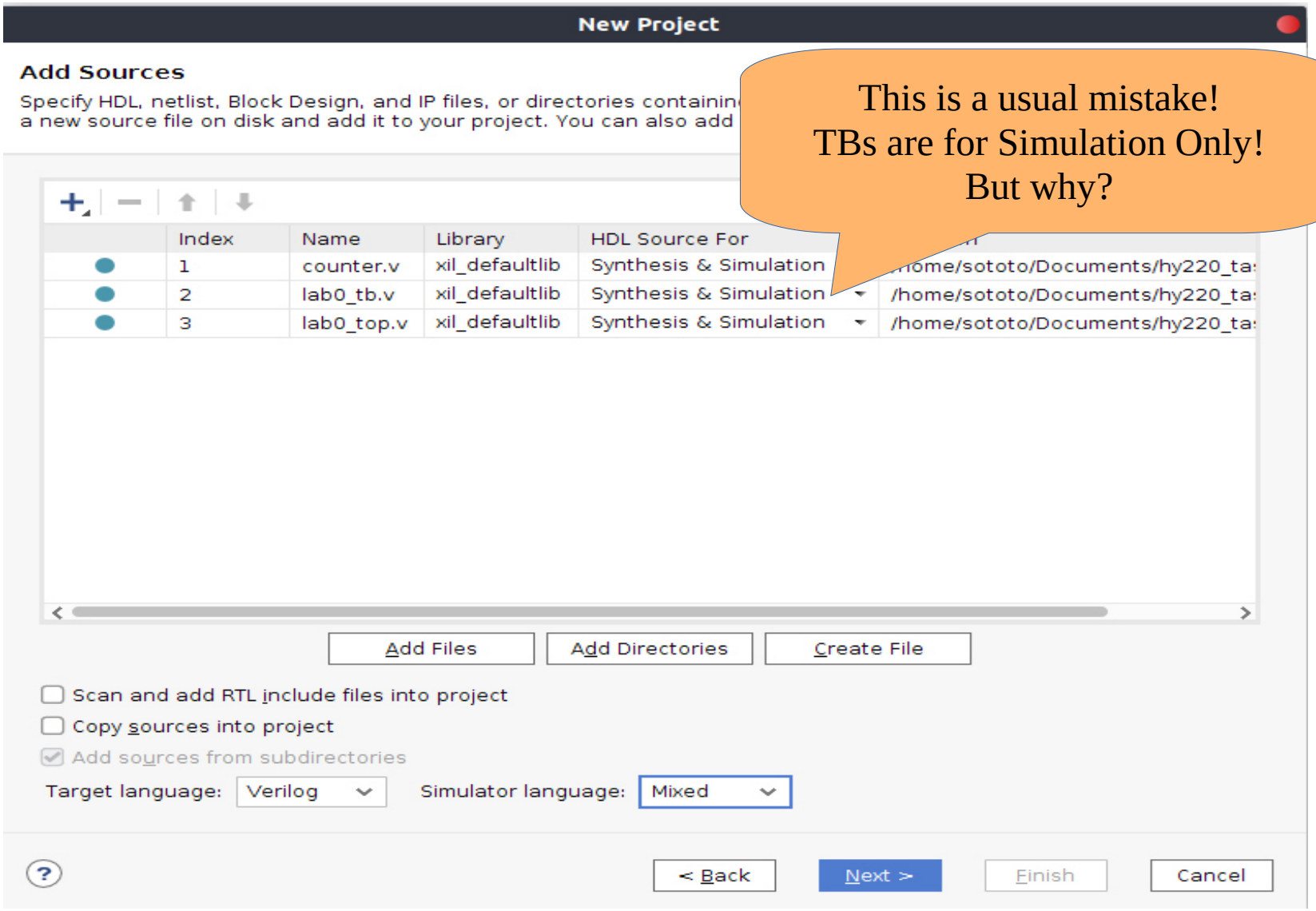
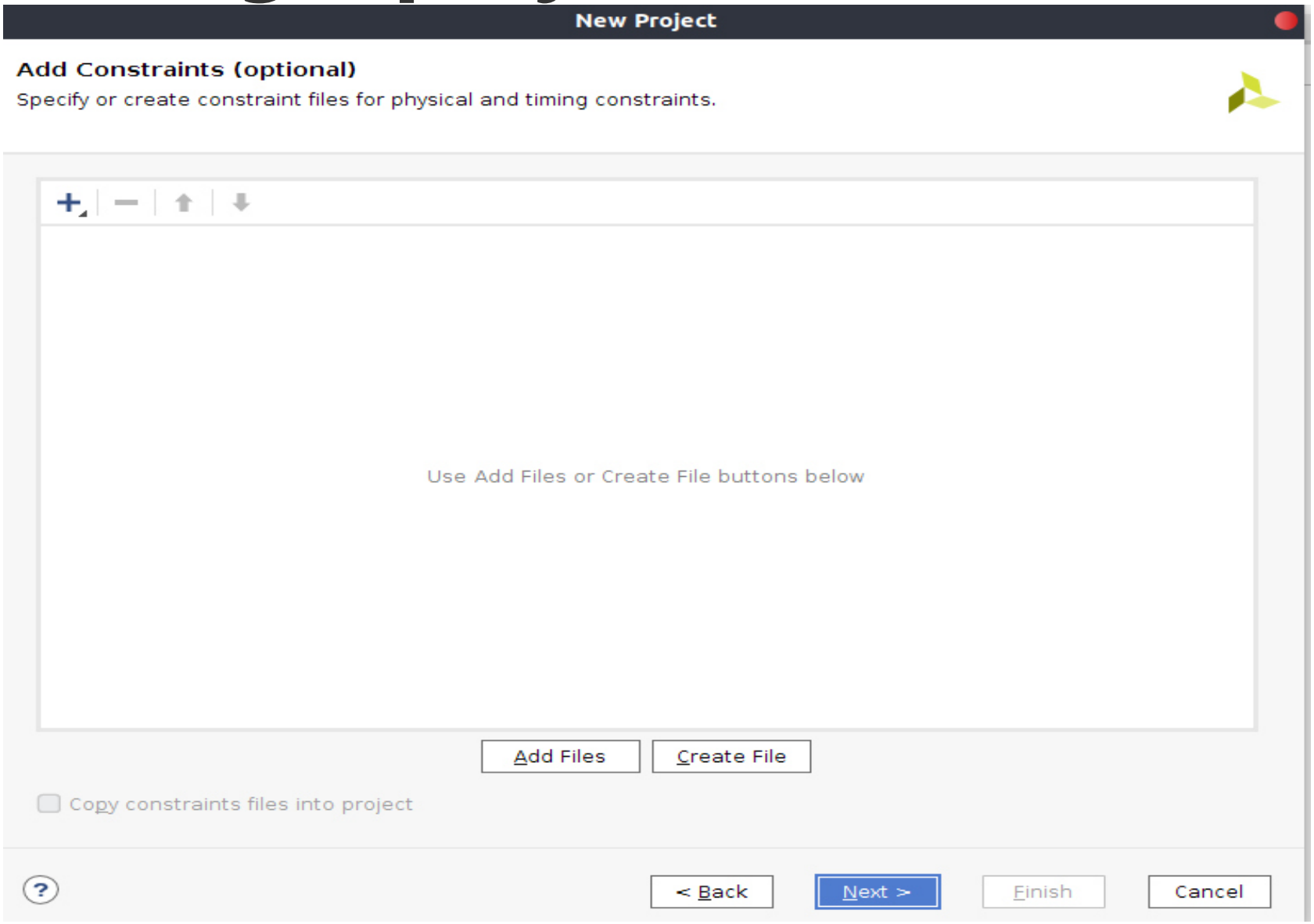


Xilinx Constraints files (XDC)

- FPGAs include some physical pins such as buttons, LEDs, etc.
- If we are planning on using these pins we must inform Vivado to associate them with our HW designs
- All XDC files are provided

Creating a project (cont'd)



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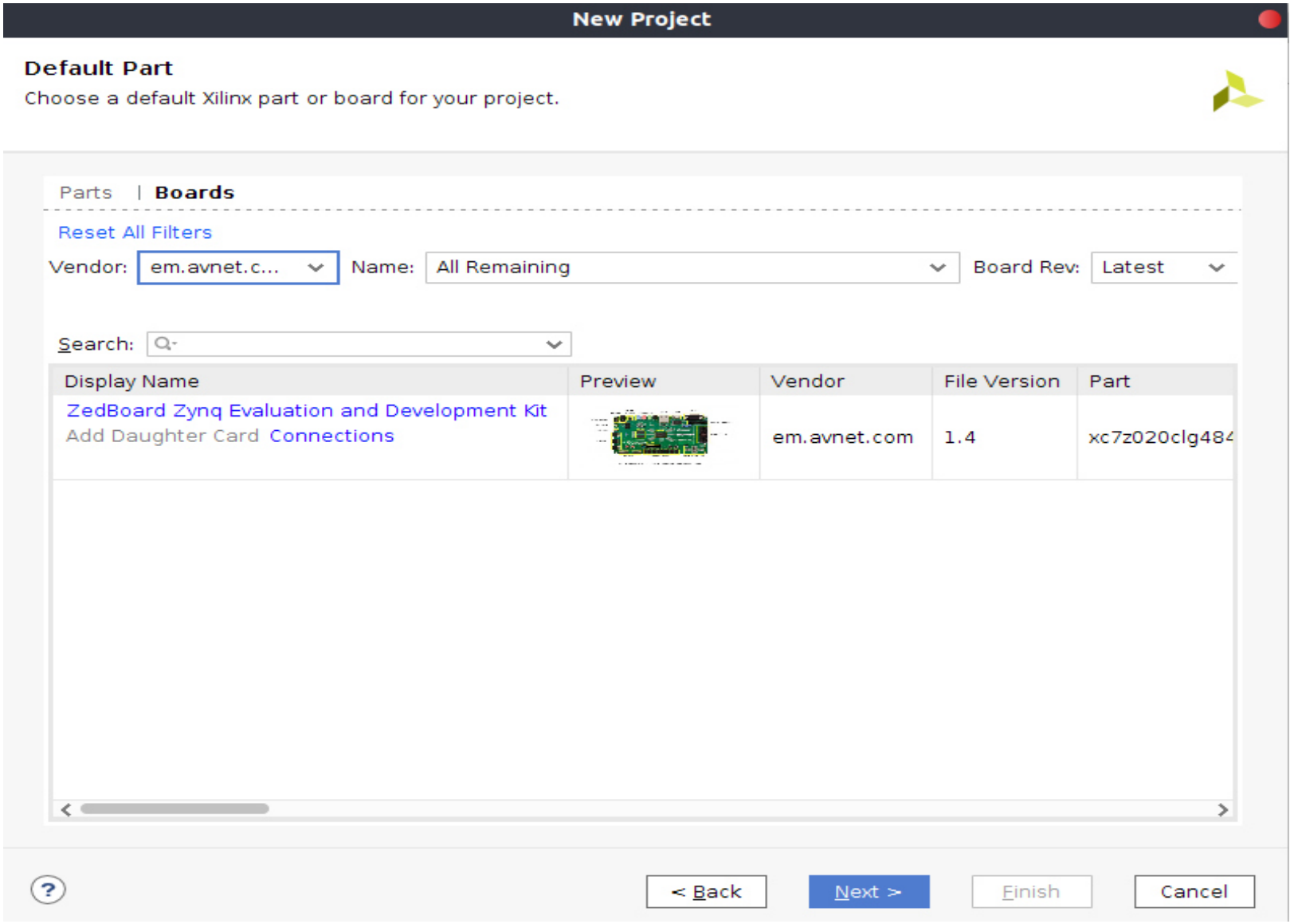

Flow Navigator

- Run Simulation
  - Shows the waveform of the design that represents its behavior
  - Main debugging routine
- Open Elaborated Design
  - Generates and displays the schematic of your design

Flow Navigator

- Run Synthesis
  - Shows the corresponding LUT schematic of the selected device
  - Displays info about timing, utilization and critical paths
- Run Implementation
  - Implements your design and places it on the selected FPGA device

Flow Navigator

- Generate bitstream
  - Generates the bitstream, which is used to program the FPGA
- Open Hardware Manager
  - Finds the connected device
  - Programs Device to download the generated bitstream to the connected device

Switch to Vivado for demo