Introduction to hardware design

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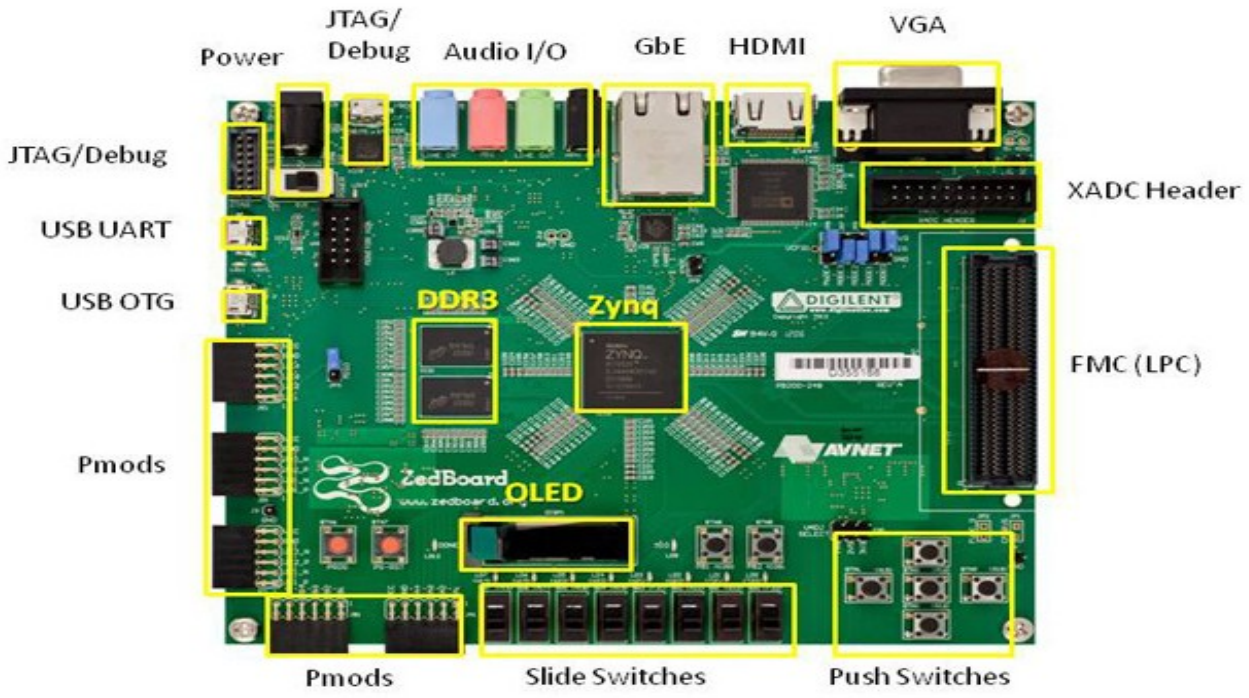
CS-220 (Spring ‘24)

FPGAs

- A Field Programmable Gate Array is a re-configurable circuit
- Hardware Description Languages (HDLs)



* SD card cage and OSPI Flash reside on backside of board

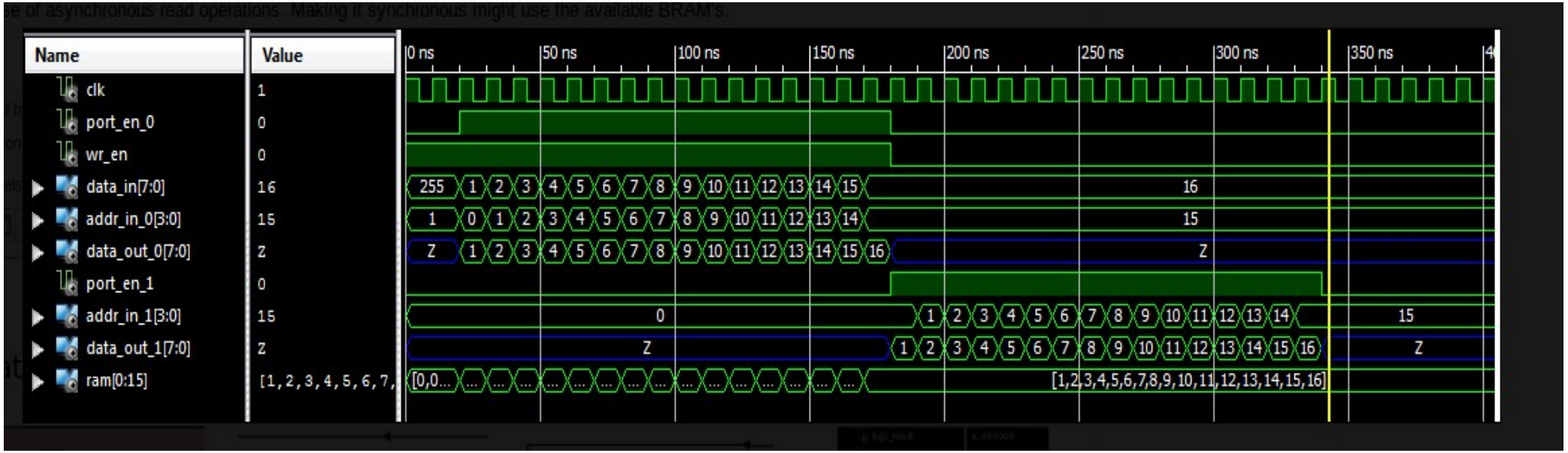
Vivado Design Suite

- Developed by Xilinx (now AMD)
- Vivado is suitable for
  - Simulation
  - Synthesis

  of HDL (SystemVerilog) designs

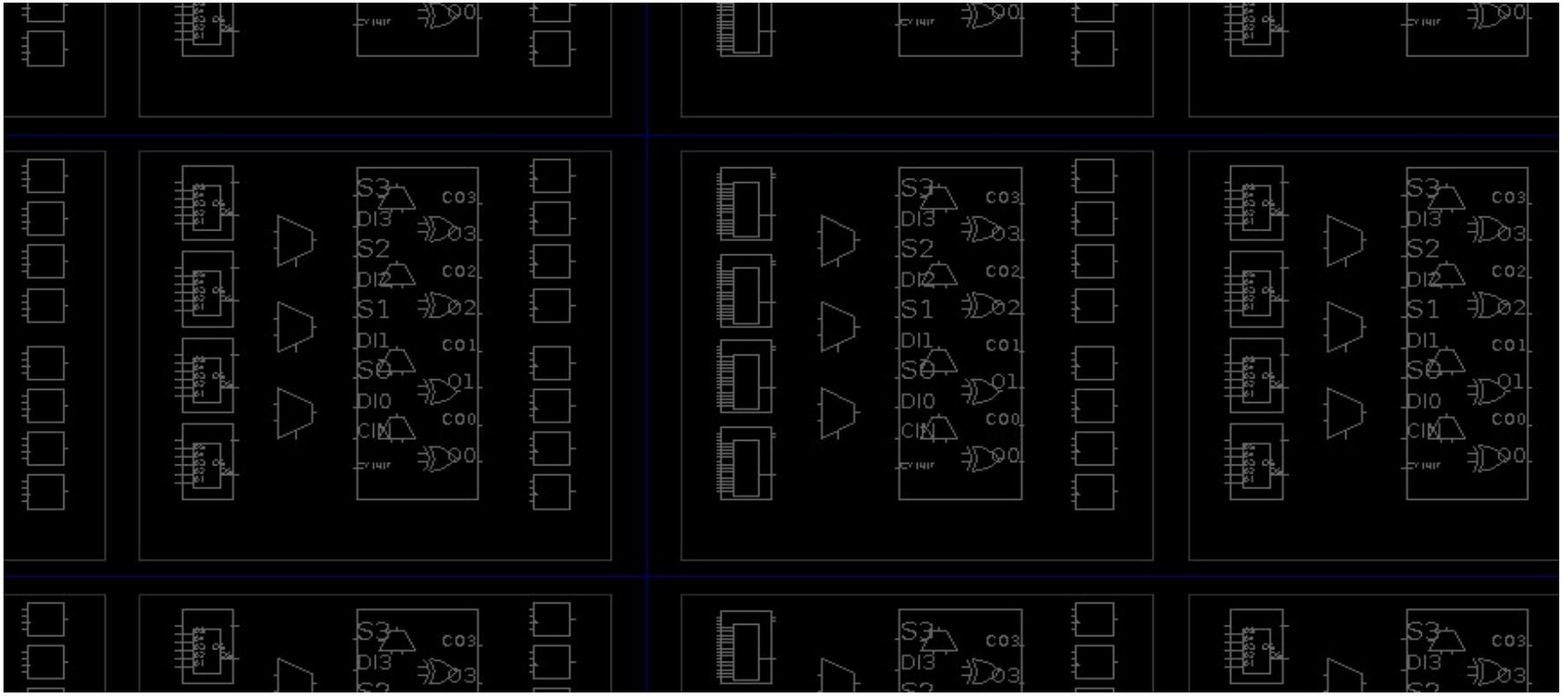
Simulation

- The simulation of a circuit displays circuit’s behavior to hardware (HW) designers
- Why do we need a testbench (TB) for that?



Synthesis

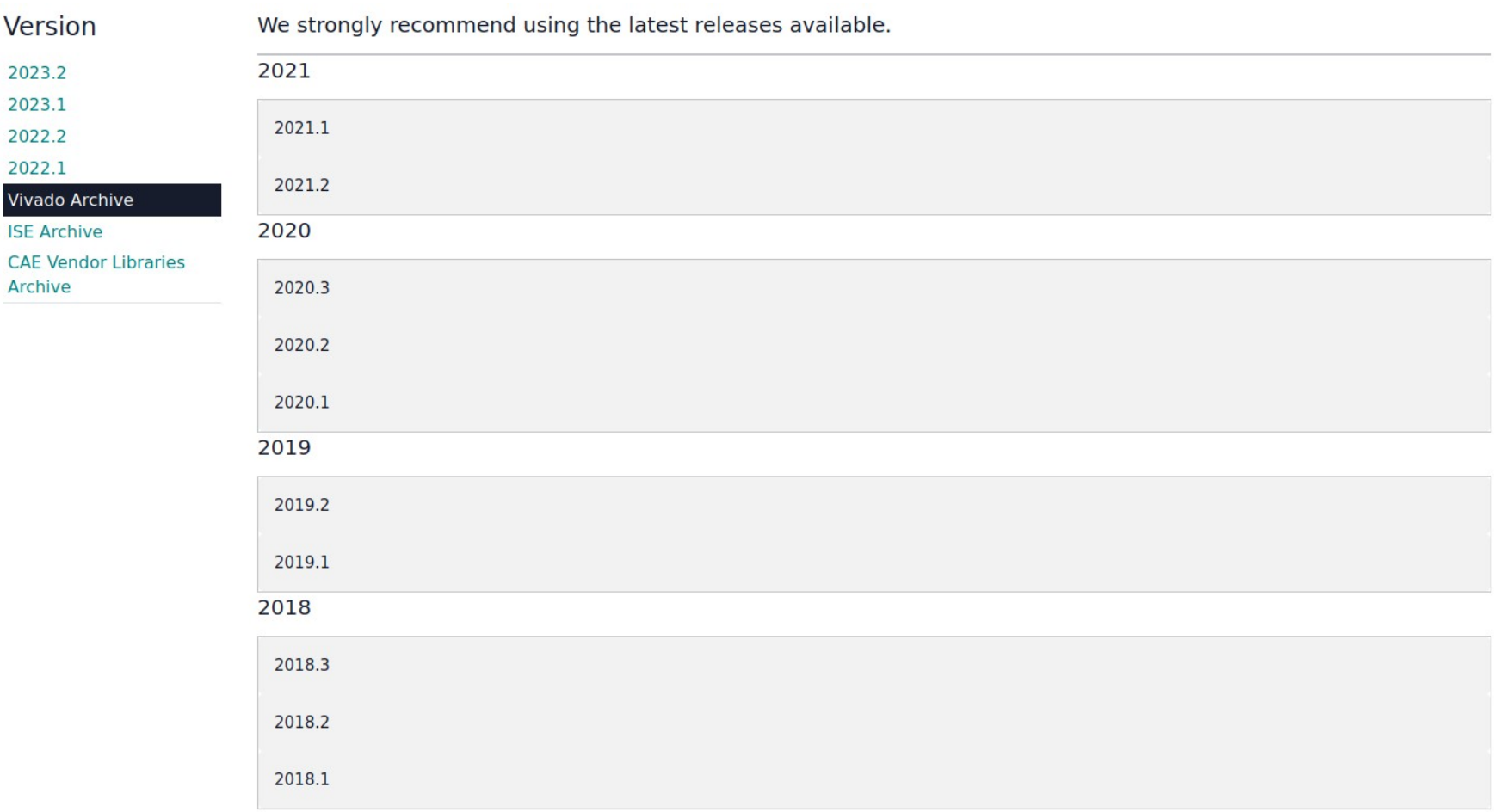
- Transforms Register Transfer Level (RTL) designs to logic gates
- Look-Up Tables (LUTs)



Vivado Installation

- Dependencies for Linux machines
  - sudo apt install libtinfo5
  - sudo apt install libncurses5
- Linux installation
  - sudo ./xsetup
- Windows installation
  - xsetup.exe

Vivado Installation (cont’d)



Vivado Installation (cont'd)

Vivado Design Suite - HLx Editions - 2018.3 Full Product Installation

Important

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see **Installer Information** for details.

Note: Download verification is only supported with Google Chrome and Microsoft Edge web bowsers.

Vivado HLx 2018.3: All OS installer Single-File Download (TAR/GZIP - 18.97 GB)

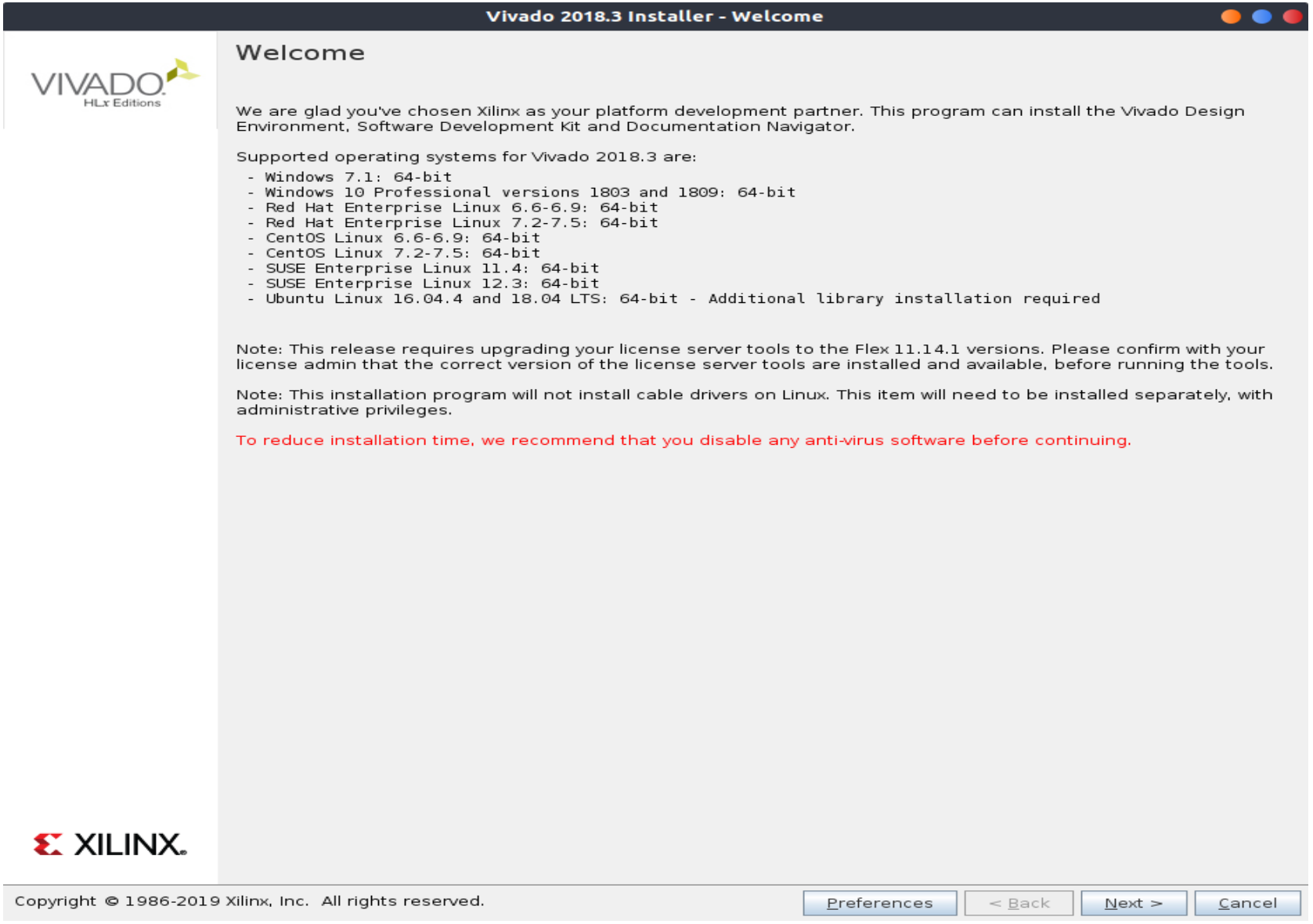
MD5 SUM Value : 8a3a75f26d0e20de21fc673ad9d40d0f

Download Verification

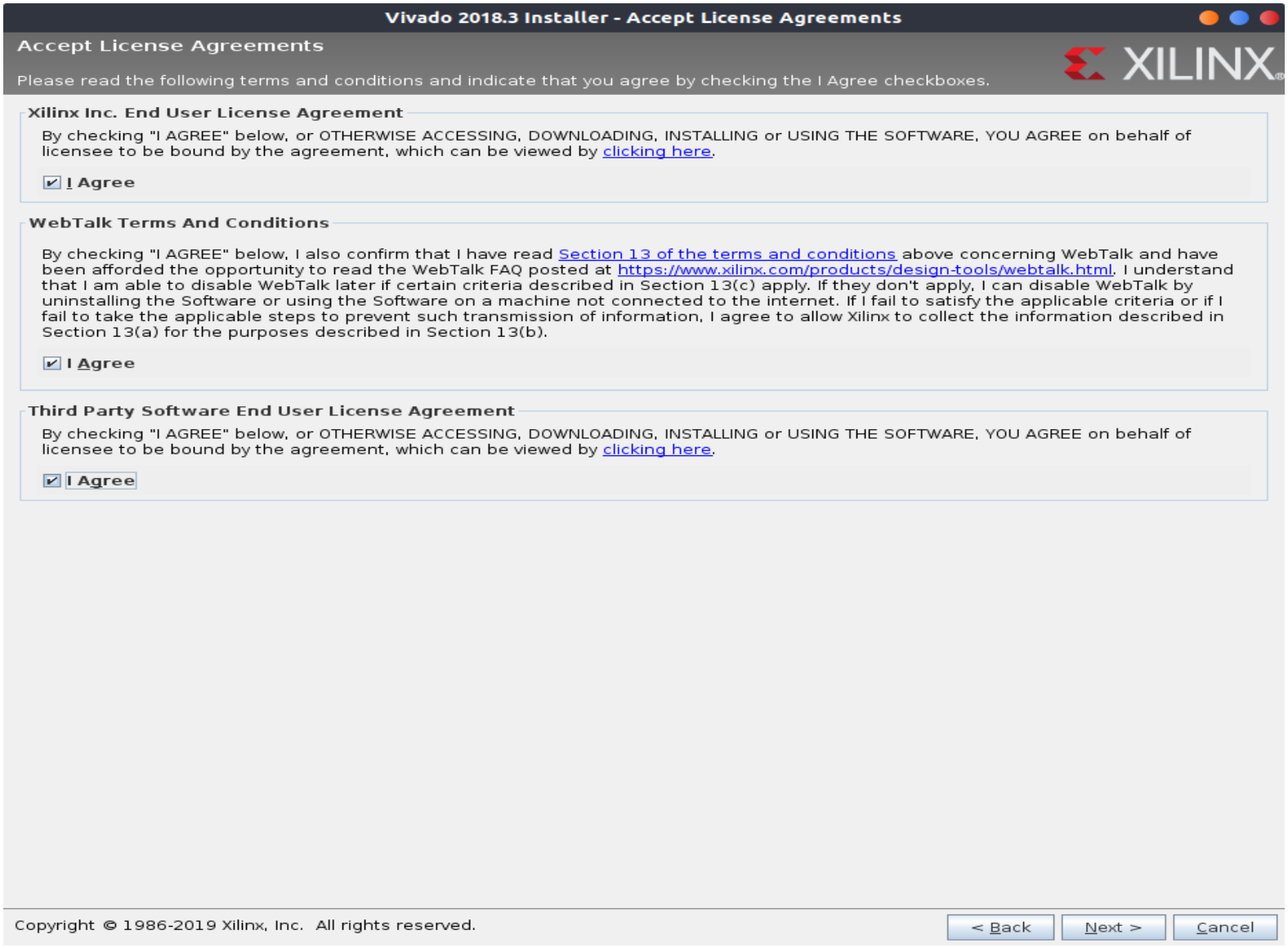
Digests | Signature | Public Key

Download Includes	Vivado Design Suite HLx Editions (All Editions)
Download Type	Full Product Installation
Last Updated	Dec 10, 2018
Answers	2018.x - Vivado Known Issues
Documentation	Release Notes
Support Forums	Installation and Licensing

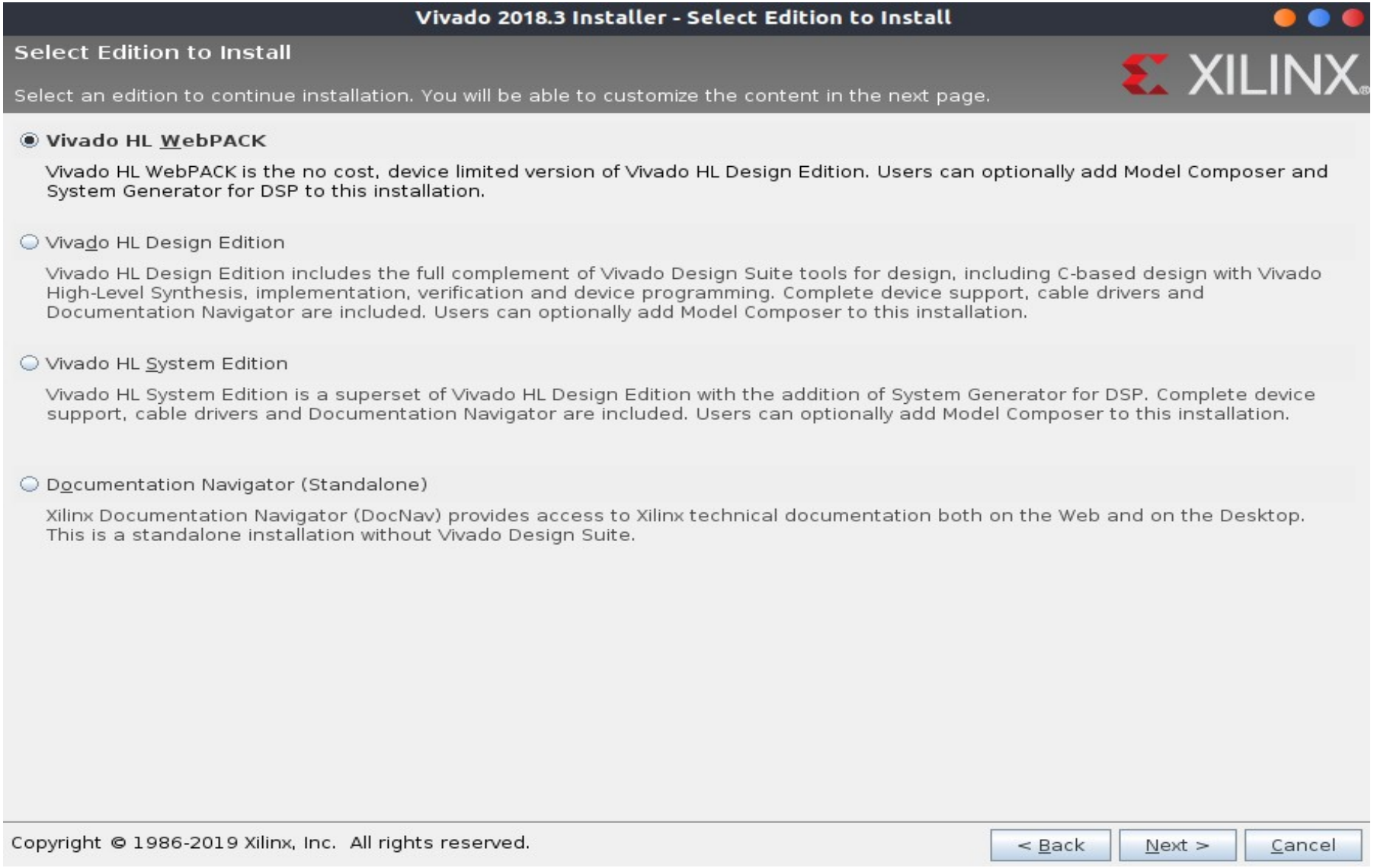
Vivado Installation (cont'd)



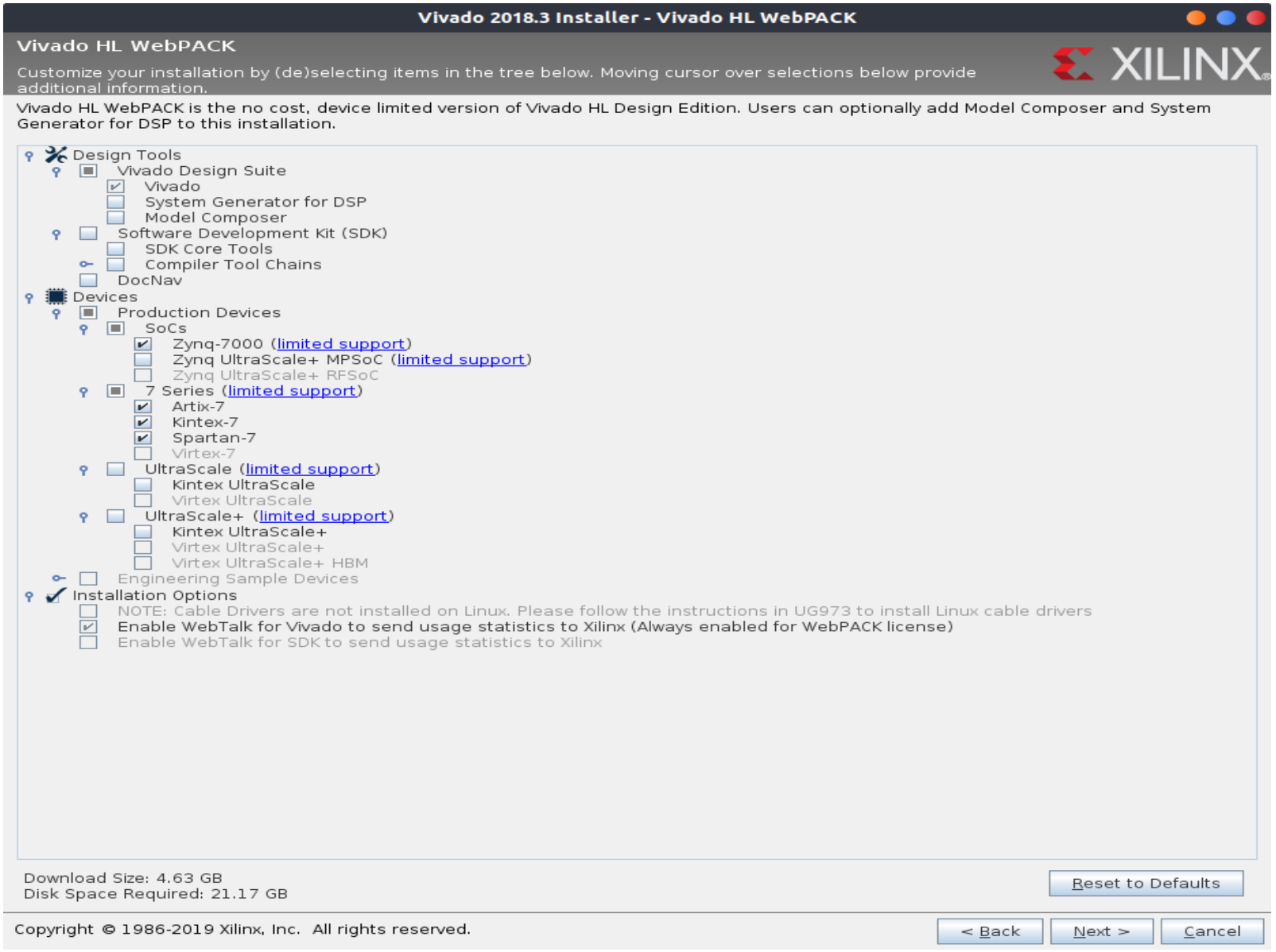
Vivado Installation (cont'd)



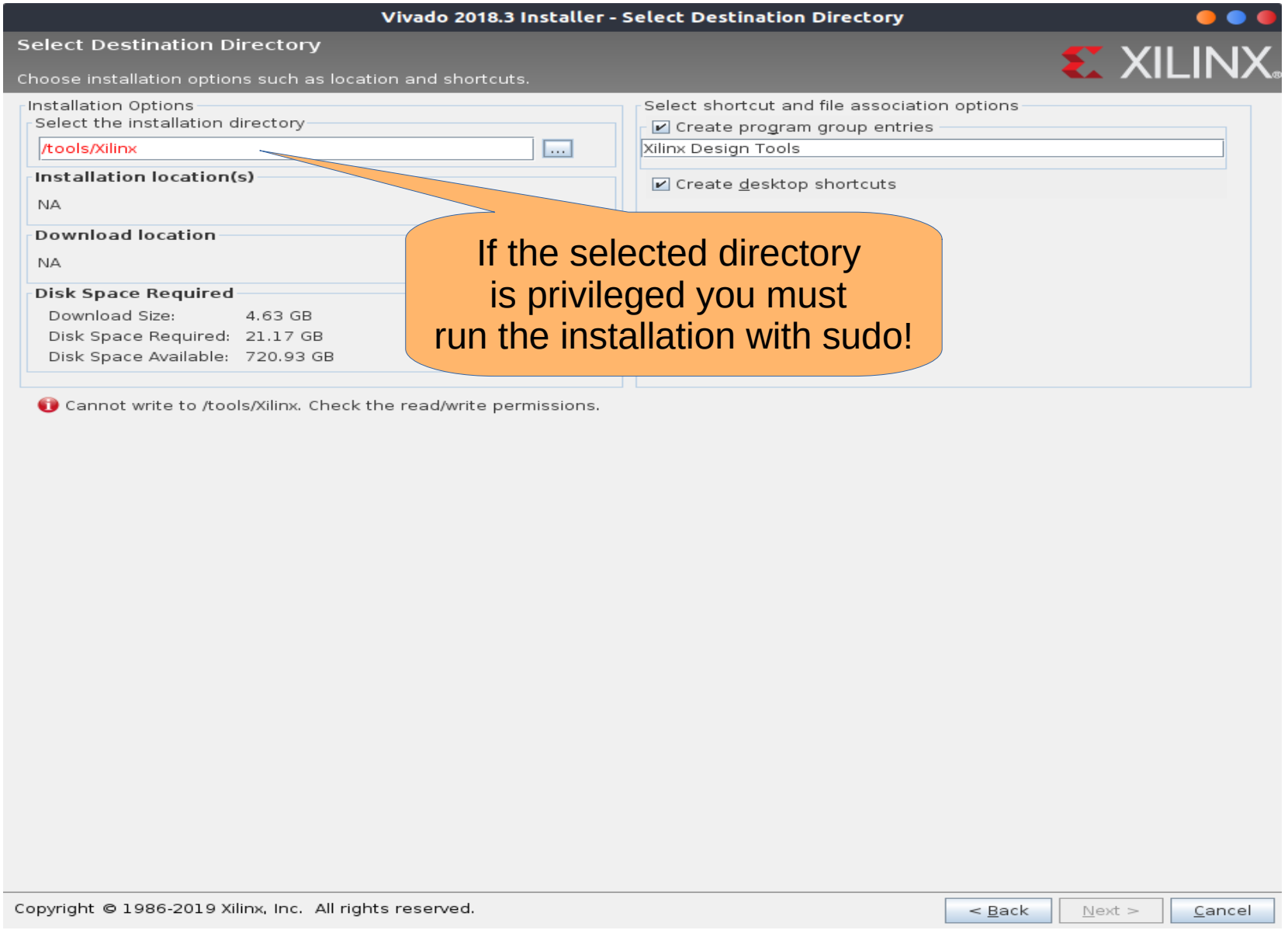
Vivado Installation (cont'd)



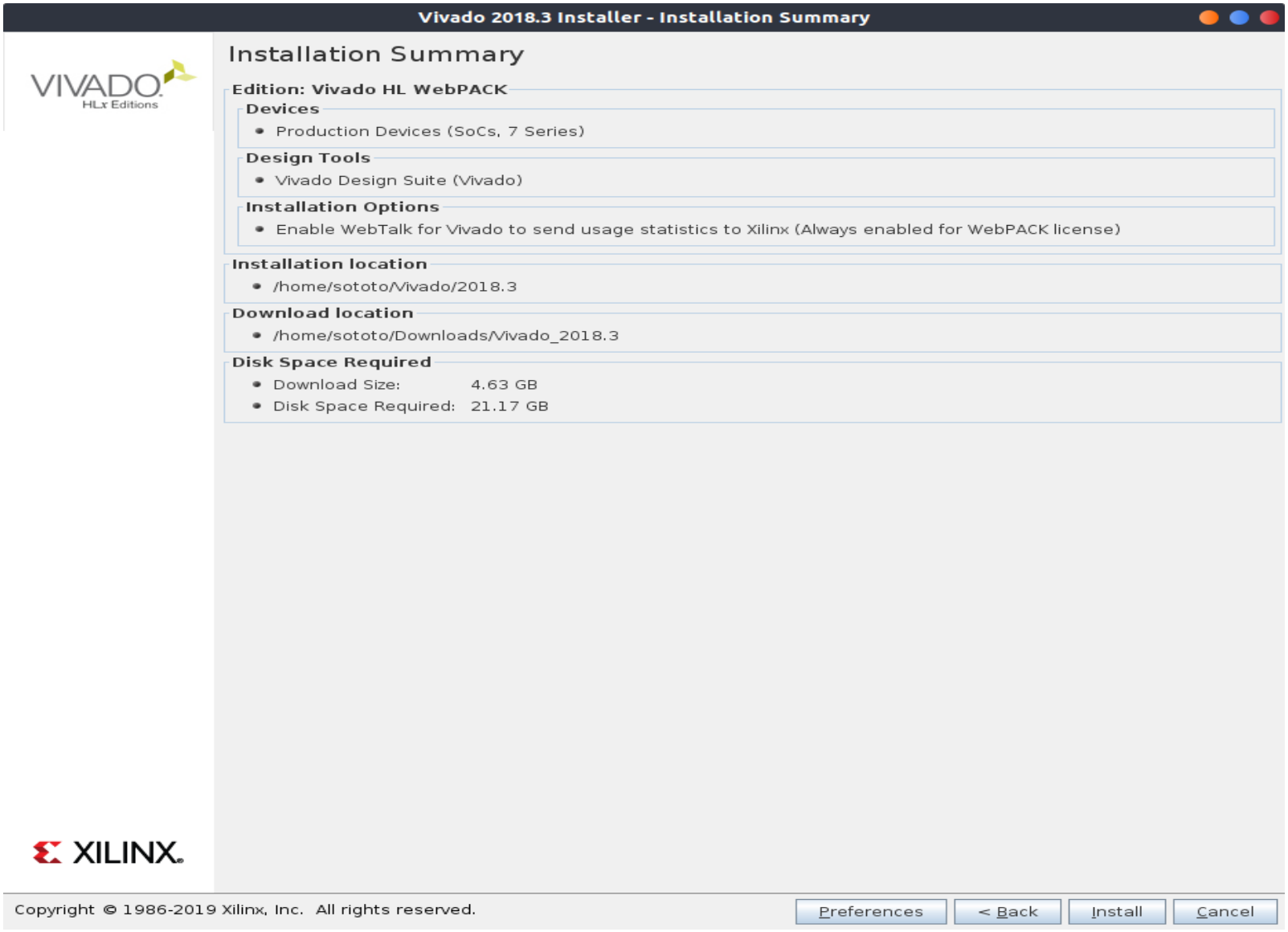
Vivado Installation (cont'd)



Vivado Installation (cont'd)



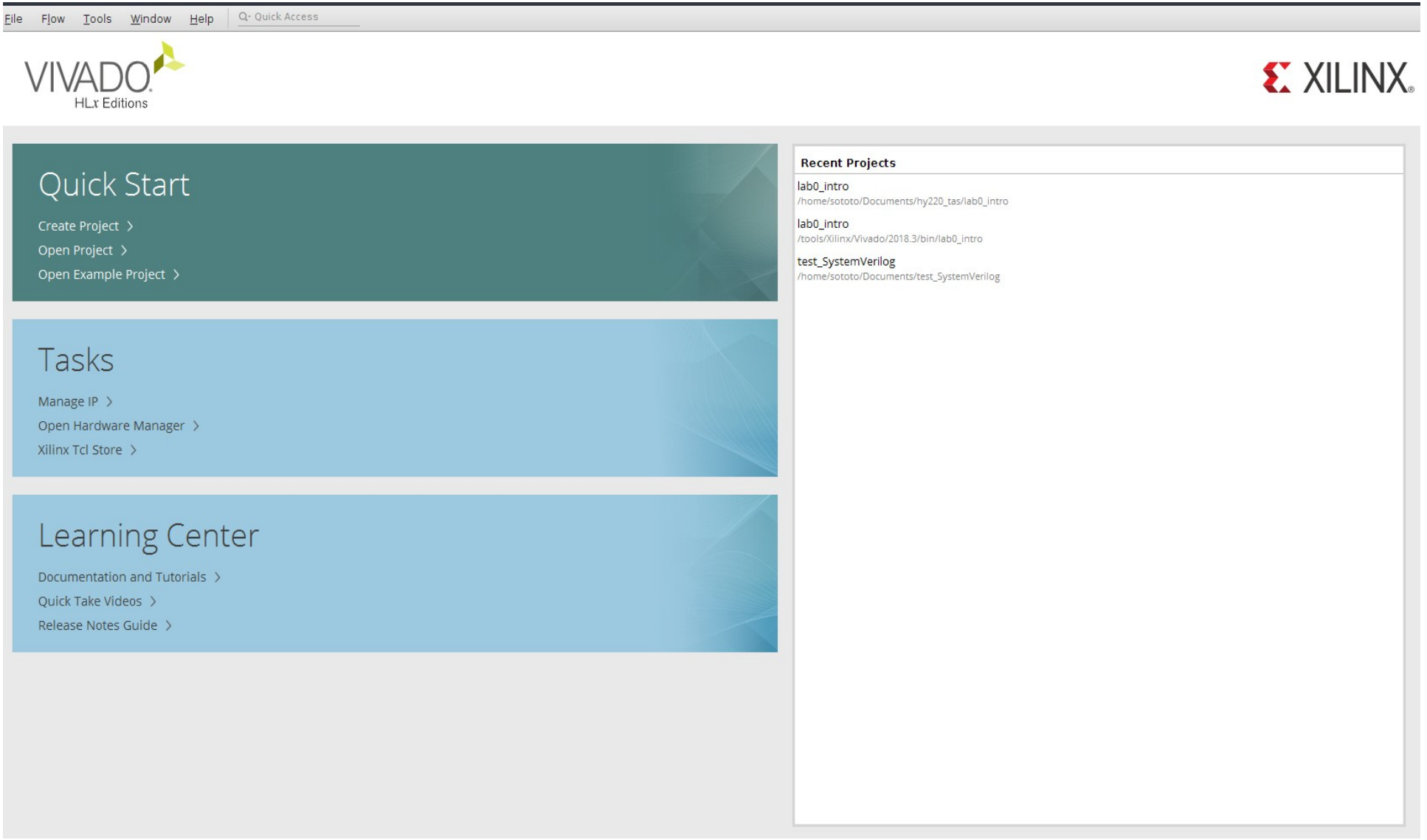
Vivado Installation (cont'd)



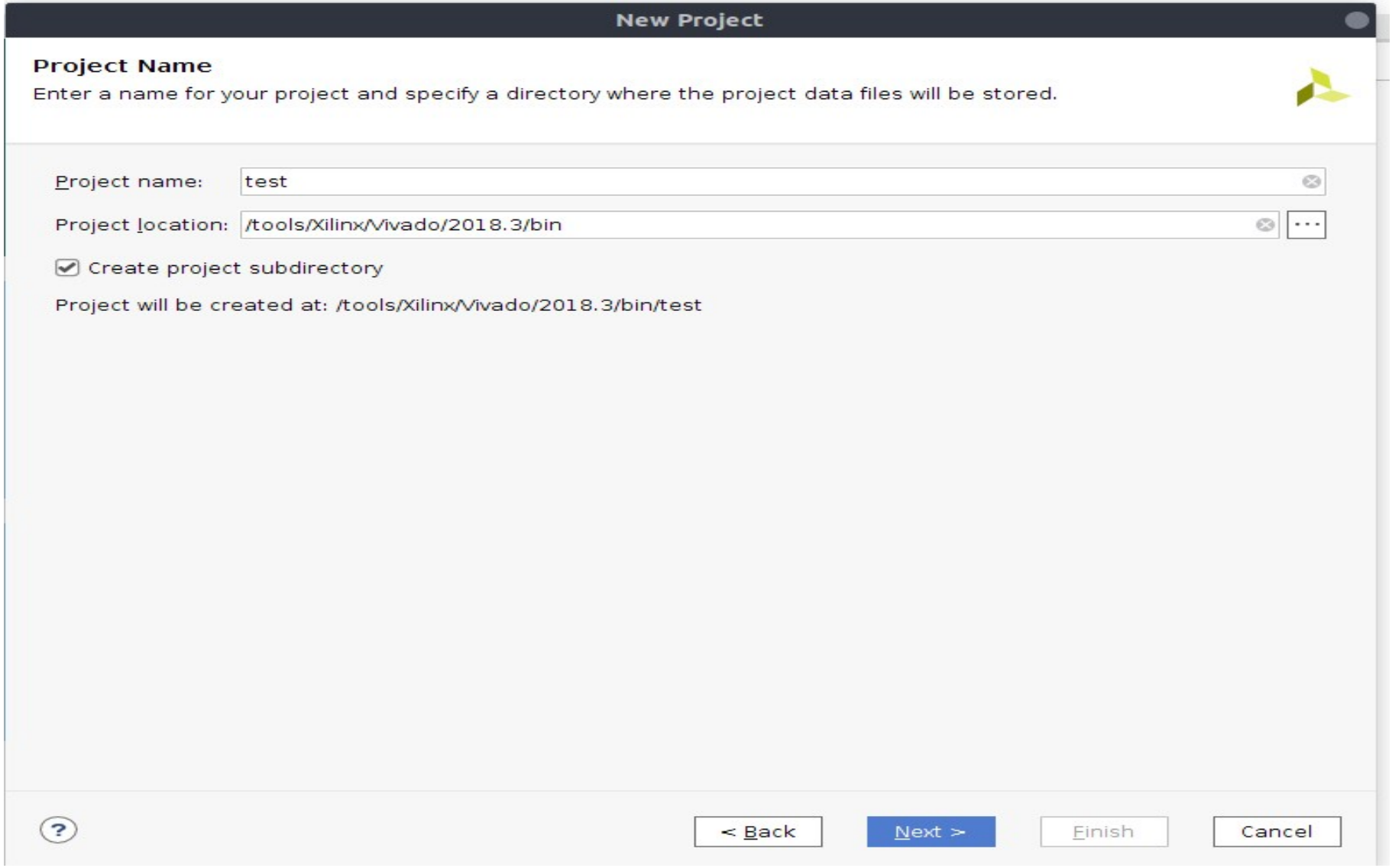
Sourcing settings to path

- Before executing Vivado through command line you have to source its settings
  - cd installation_path/Xilinx/Vivado/2018.3
  - source settings64.sh
- After this you can execute Vivado GUI by typing
  - vivado

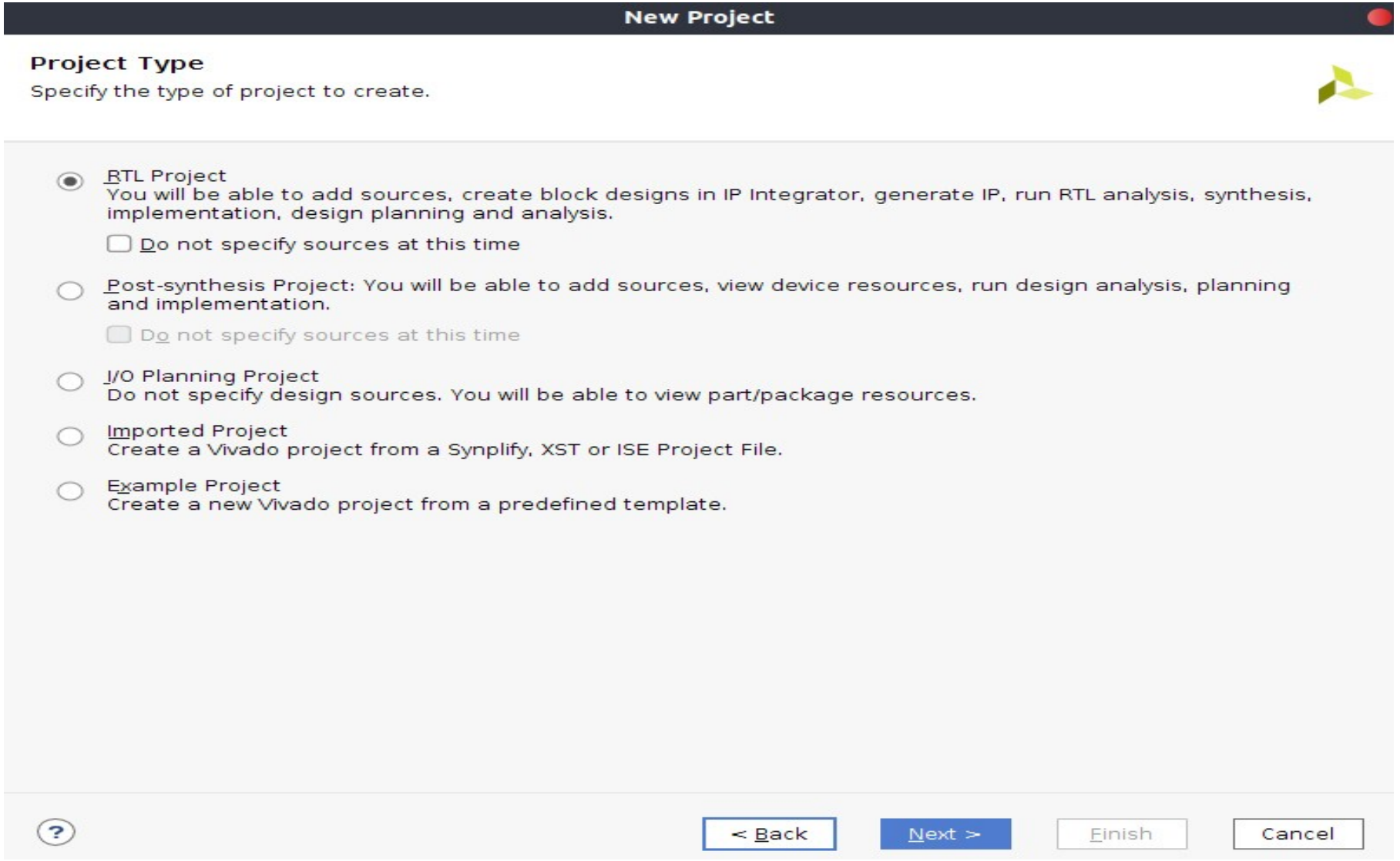
Creating a project



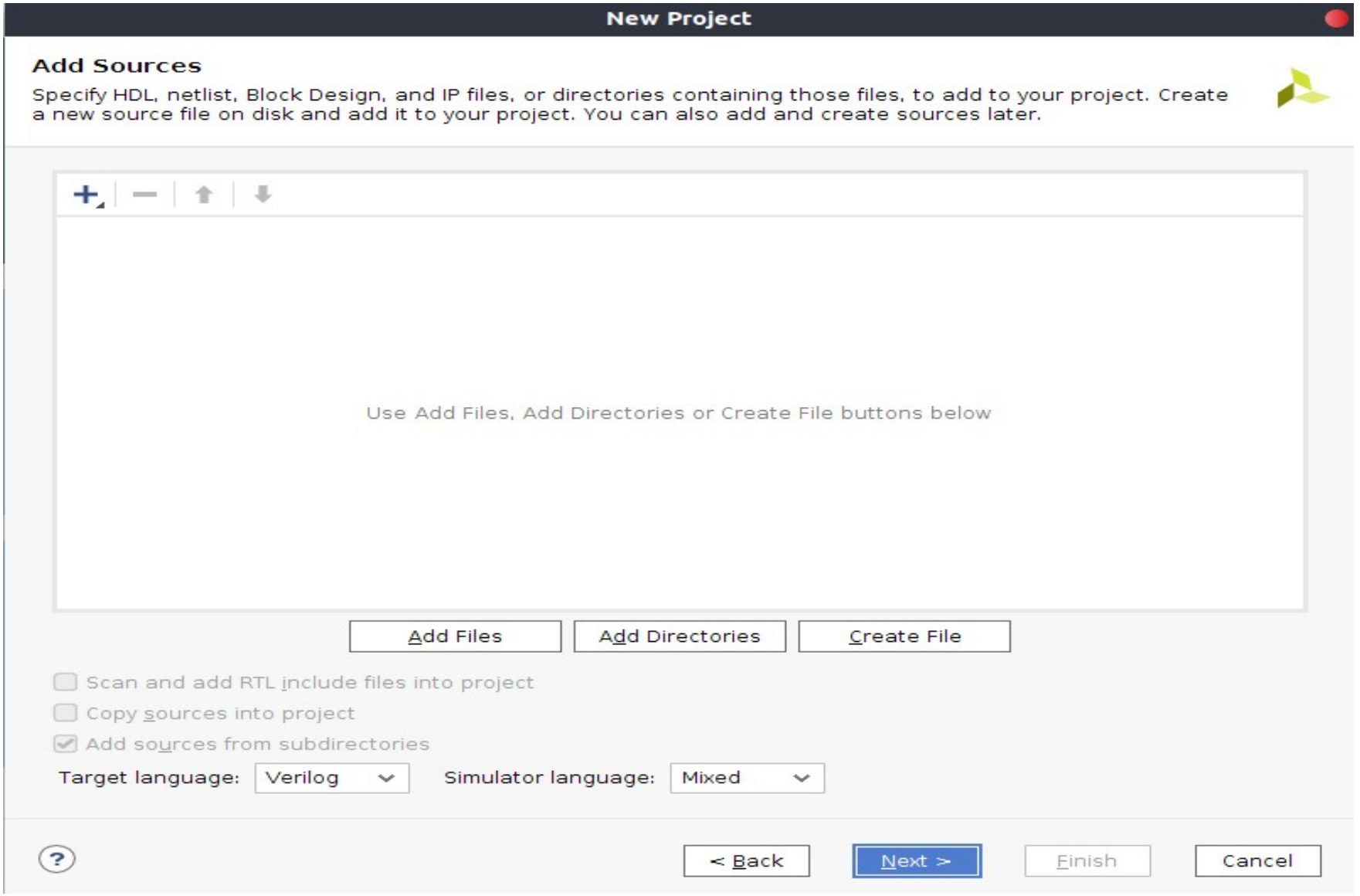
Creating a project (cont’d)



Creating a project (cont'd)



Creating a project (cont'd)



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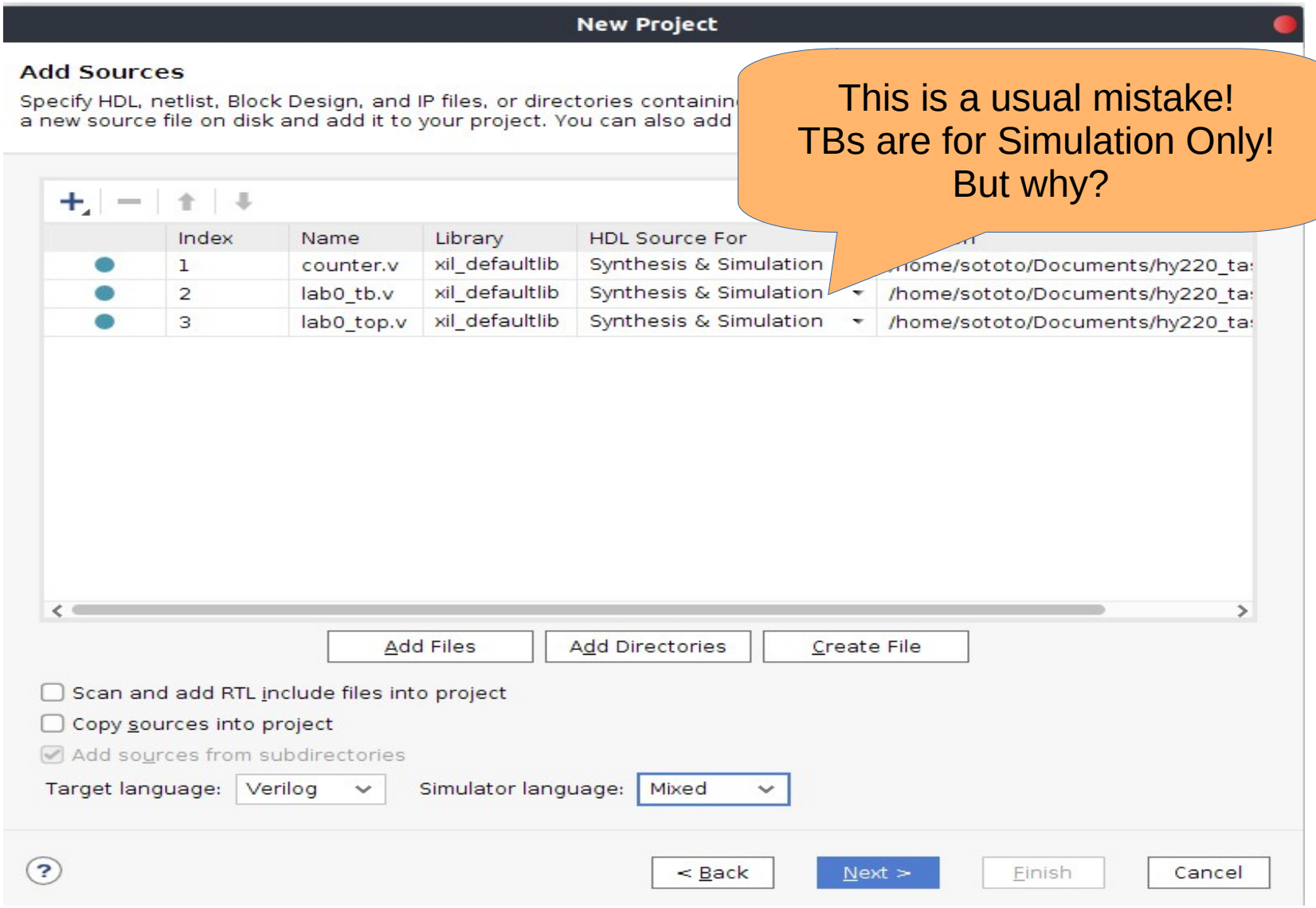
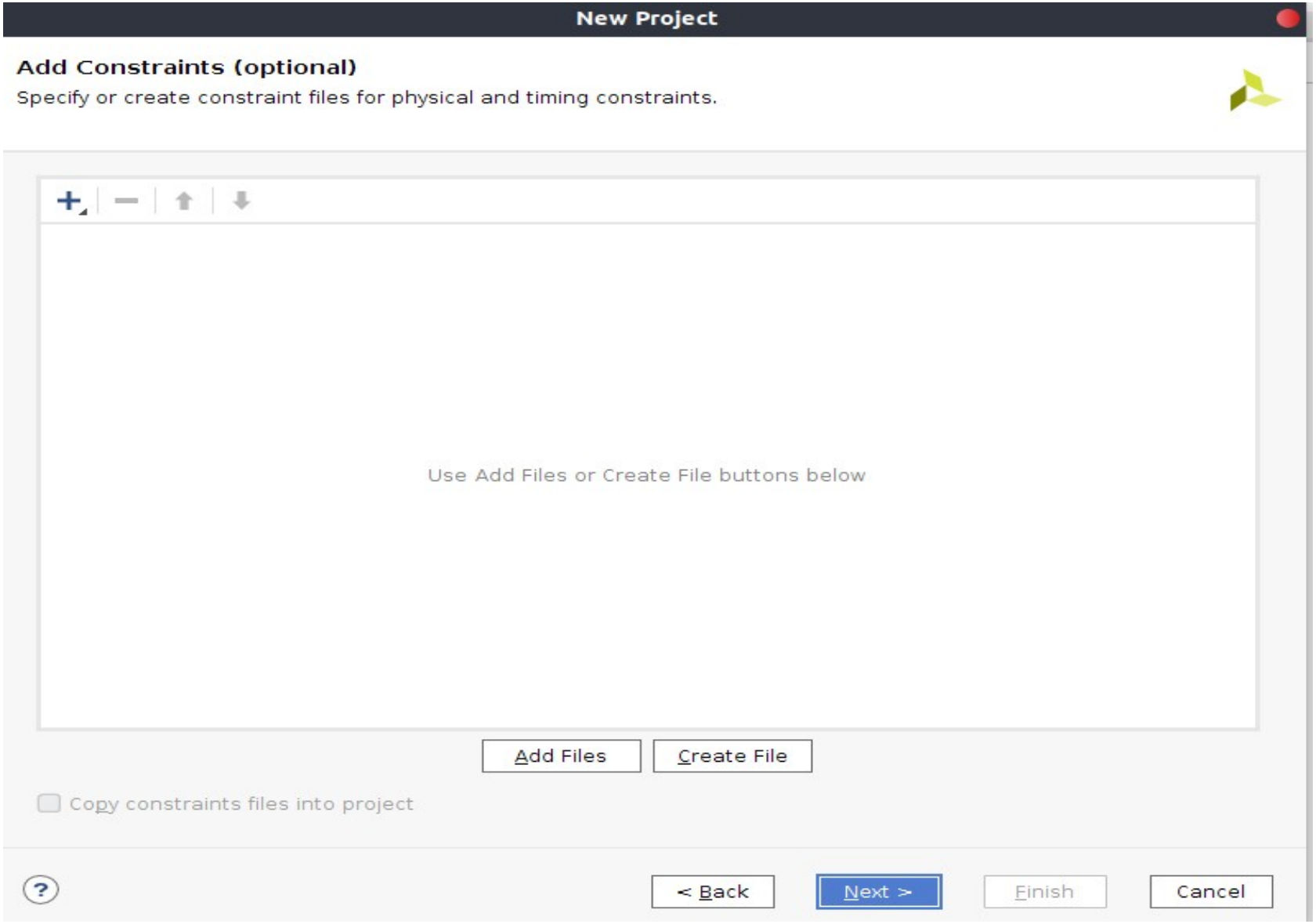


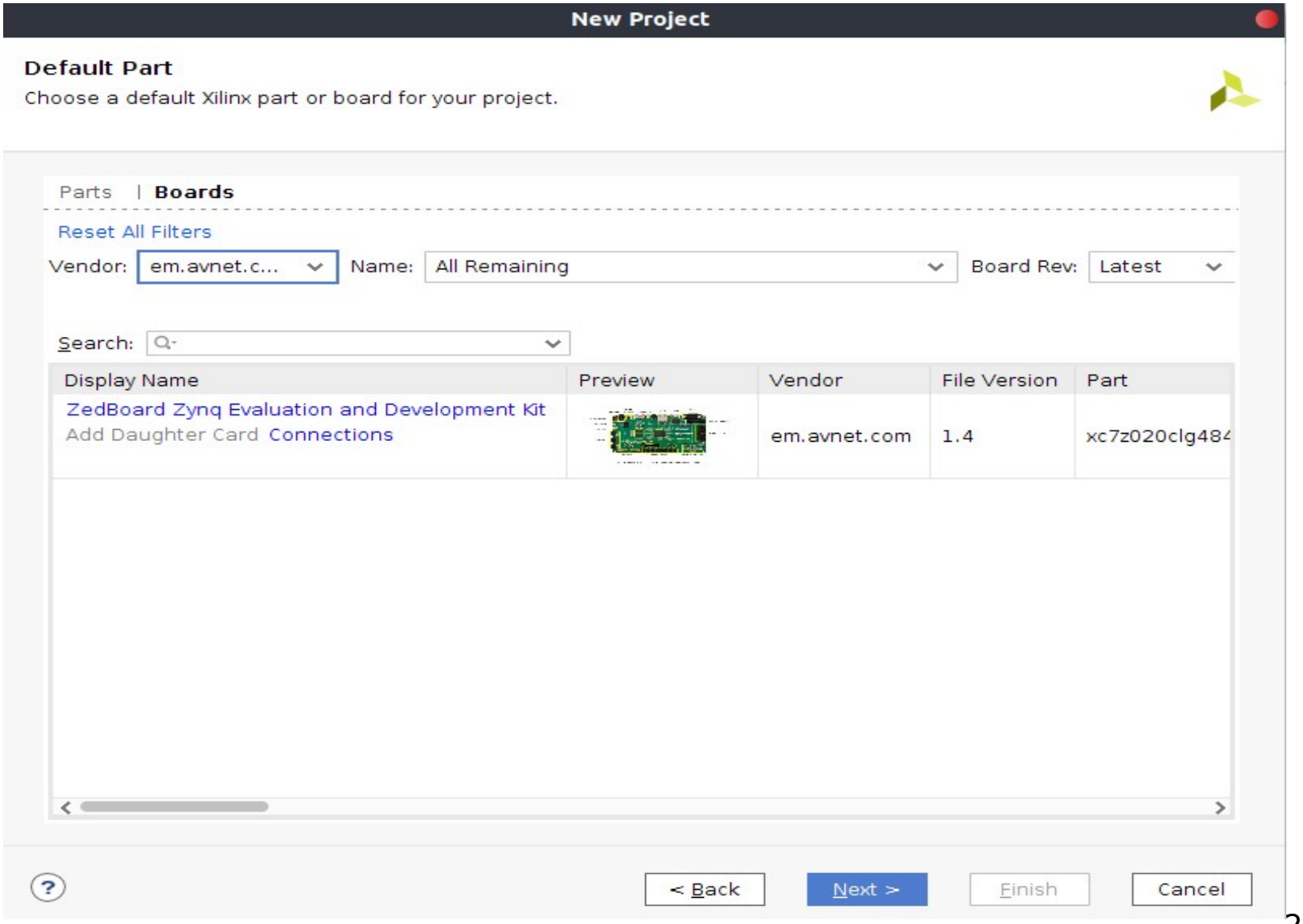
Xilinx Constraints files (XDC)

- FPGAs include some physical pins such as buttons, LEDs, etc.
- If we are planning on using these pins we must inform Vivado to associate them with our HW designs
- All XDC files are provided

Creating a project (cont'd)



Creating a project (cont'd)



Flow Navigator

- Run Simulation
  - Shows the waveform of the design that represents its behavior
  - Main debugging routine
- Open Elaborated Design
  - Generates and displays the schematic of your design

Flow Navigator

- Run Synthesis
  - Shows the corresponding LUT schematic of the selected device
  - Displays info about timing, utilization and critical paths
- Run Implementation
  - Implements your design and places it on the selected FPGA device

Flow Navigator

- Generate bitstream
  - Generates the bitstream, which is used to program the FPGA
- Open Hardware Manager
  - Finds the connected device
  - Programs Device to download the generated bitstream to the connected device

Work remotely - connect

- Instead of working on your own machine, you can run simulations on Debian machines.
  - Interactively through command line
  - Interactively with GUI through ssh display forwarding (ssh -X <hostname>)

Work remotely – flow

- cp -r ~hy220/tools/example .
- cd example
- source setup.sh
- export HY220_SIMULATOR=[verilator,vivado,icarus]
- Work interactively
  - make
  - make gwaves (after make)
    - It opens the generated wave files with gtkwave viewer

Work remotely – your files

- mkdir project_file
- cp Makefile, setup.sh (from example)
- Edit Makefile (SRCS, TOP_MODULE)
- Repeat compilation flow

Switch to Vivado for demo